THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)
Mecheri, Salem - 636 453.

Approved by AICTE, New Delhi
Affiliated to Anna University

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

AUTONOMOUS
CURRICULUM AND

PG
REGULATIONS
2024
Academic Year 2024-25 onwards

SYLLABUS
I - IV
SEMESTERS

M.E. APLLIED ELECTRONICS
CHOICE BASED CREDIT SYSTEM
CURRICULUM FOR SEMESTER I TO IV

(Applicable to the students admitted from the Academic year 2024-2025 onwards)

VISION

- To be a centre of excellence in education, training and research in Electronics and Communication Engineering to cultivate technically competent professionals for Industry and Society.

MISSION

- To import knowledge and skills to face challenges in Electronics and Communication Engineering.
- To provide ethical value based education to address the social needs.
- To provide innovative environment to learning global atonements.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

Our Graduates will have

- To enable graduates to develop solutions to real world problems in the frontier areas of Applied Electronics.
- To enable the graduates to adapt to the latest trends in technology through self- learning and to pursue research to meet out the demands in industries and Academia.
- To enable the graduates to exhibit leadership skills and enhance their abilities through lifelong learning.
- To become entrepreneurs to develop indigenous solutions.

PROGRAMME OUTCOMES (POs)

- An ability to independently carry out research/investigation and development work to solve practical problems
- An ability to write and present a substantial technical report/document
- Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
- To critically evaluate the design and provide optimal solutions to problem areas in advanced signal processing, Consumer and automotive systems, embedded systems and VLSI design.

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- To enhance and develop electronic systems, protocols between circuits using modern engineering hardware and software tools.
- To acquire knowledge of fundamentals of power electronics, power management, wireless, power supply circuits, RF circuits and FPGA circuits

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REGULATIONS - 2024

CHOICE BASED CREDIT SYSTEM

M.E. APPLIED ELECTRONICS

CURRICULUM & SYLLABI FOR I TO IV SEMESTERS

SEMESTER – I

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			Category
		L	T	P		CA	ESE	Total	
Theory/Theory with Practical									
PAMAET2411	Applied Mathematics for Electronics Engineers	3	1	0	4	40	60	100	FC
PRMT2411	Research Methodology and IPR	2	0	0	2	40	60	100	RMC
PAPT2401	Advanced Digital Signal Processing	3	0	0	3	40	60	100	PCC
PAPT2402	Advanced Digital System Design	3	0	2	4	50	50	100	PCC
PAPT2403	Semiconductor Devices and Modeling	3	0	0	3	40	60	100	PCC
PAPT2404	Digital CMOS VLSI Design	3	0	0	3	40	60	100	PCC
	Audit Course I*	2	0	0	0				AC
Practical / Employability Enhancement									
PAPL2401	Electronics System Design Laboratory	0	0	3	1.5	60	40	100	PCC
PAPL2402	Signal Processing Laboratory	0	0	3	1.5	60	40	100	PCC
	Total Credits to be earned				**22**				

* Audit Course is optional # For Students admitted from 2025 year onwards.

SEMESTER – II

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			Category
		L	T	P		CA	ESE	Total	
Theory/Theory with Practical									
PAPT2421	Analog and Mixed Signal IC Design	3	0	0	3	40	60	100	PCC
PAPT2422	Industrial Internet of Things	3	0	0	3	40	60	100	PCC
PAPT2423	Power Conversion Circuits for Electronics	3	0	0	3	40	60	100	PCC
PAPT2424	Embedded Systems	3	0	2	4	50	50	100	PCC
	Professional Elective I	3	0	0	3	40	60	100	PEC
	Professional Elective II	3	0	0	3	40	60	100	PEC
	Audit Course II*	2	0	0	0				AC
Practical / Employability Enhancement									
PAPL2421	VLSI Design Laboratory	0	0	4	2	60	40	100	PCC
PAPL2422	Mini Project with seminar	0	0	2	1	60	40	100	EEC
	Total Credits to be earned				**22**				

* Audit Course is optional

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SEMESTER – III									
Course Code	Course Title	Hours / Week			Credit	Maximum Marks			Category
		L	T	P		CA	ESE	Total	
Theory/Theory with Practical									
	Professional Elective III	3	0	0	3	40	60	100	PEC
	Professional Elective IV	3	0	0	3	40	60	100	PEC
	Professional Elective V	3	0	2	4	50	50	100	PEC
	Open Elective	3	0	0	3	40	60	100	OEC
Practical / Employability Enhancement									
PAPL2431	Project Work I	0	0	12	6	60	40	100	EEC
PAPL2432	Internship	0	0	0	1	100	-	100	EEC
Total Credits to be earned					20				

SEMESTER – IV									
Course Code	Course Title	Hours / Week			Credit	Maximum Marks			Category
		L	T	P		CA	ESE	Total	
Practical / Employability Enhancement									
PAPL2441	Project Work II	0	0	24	12	60	40	100	PCC
Total Credits to be earned					12				

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AUDIT COURSES

Course Code	Course Title	Hours / Week			Contact periods
		L	T	P	
Theory/Theory with Practical					
PAXC2401	Constitution of India	2	0	0	0
PAXC2402	English for Research Paper Writing	2	0	0	0
PAXC2403	Disaster Management	2	0	0	0
PAXC2404	நற்றமிழ் இலக்கியம்	2	0	0	0

PROFESSIONAL ELECTIVES

SEMESTER II, ELECTIVE I

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	PAPE2401	Applications Specific Integrated Circuits	PEC	3	0	0	3	3
2.	PAPE2402	Computer Architecture and Parallel Processing	PEC	3	0	0	3	3
3.	PAPE2403	Automotive Electronics	PEC	3	0	0	3	3
4.	PAPE2404	Robotics	PEC	3	0	0	3	3
5.	PAPE2405	Soft Computing and Optimization Techniques	PEC	3	0	0	3	3

SEMESTER II, ELECTIVE II

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	PAPE2406	RF System Design	PEC	3	0	0	3	3
2.	PAPE2407	Electromagnetic Interference and Compatibility	PEC	3	0	0	3	3
3.	PAPE2408	VLSI Design Techniques	PEC	3	0	0	3	3
4.	PAPE2409	Nano Technologies	PEC	3	0	0	3	3
5.	PAPE2410	VLSI Testing	PEC	3	0	0	3	3
6.	PAPE2411	Edge Analytics and Internet of Things	PEC	3	0	0	3	3

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SEMESTER III, ELECTIVE III

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	PAPE2412	Quantum Computing	PEC	3	0	0	3	3
2.	PAPE2413	VLSI for Wireless Communication	PEC	3	0	0	3	3
3.	PAPE2414	Micro Electro Mechanical Systems	PEC	3	0	0	3	3
4.	PAPE2415	Hardware Secure Computing	PEC	3	0	0	3	3
5.	PAPE2416	CAD for VLSI Design	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE IV

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	PAPE2417	Sensors and Actuators	PEC	3	0	0	3	3
2.	PAPE2418	Signal Integrity for High Speed Design	PEC	3	0	0	3	3
3.	PAPE2419	Consumer Electronics	PEC	3	0	0	3	3
4.	PAPE2420	Advanced Microprocessors and Microcontrollers Architectures	PEC	3	0	0	3	3
5.	PAPE2421	Biomedical Signal Processing	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE V

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	PAPE2422	Modeling and Synthesis with HDL	PEC	3	0	2	5	4
2.	PAPE2423	Deep Learning	PEC	3	0	2	5	4
3.	PAPE2424	Advanced Digital Image Processing	PEC	3	0	2	5	4
4.	PAPE2425	PCB Design	PEC	3	0	2	5	4

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LIST OF OPEN ELECTIVES FOR PG PROGRAMMES

SL. NO.	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS
			L	T	P	
1.	POE2401	IPR, Biosafety and Entrepreneurship	3	0	0	3
2.	POE2405	Machine Learning and Deep Learning	3	0	0	3
3.	POE2406	IoT for Smart Systems	3	0	0	3
4.	POE2408	Cloud Computing Technologies	3	0	0	3
5.	POE2409	Principles of Multimedia	3	0	0	3
6.	POE2413	Sustainable Management	3	0	0	3
7.	POE2414	Micro and Small Business Management	3	0	0	3
8.	POE2415	Intellectual Property Rights	3	0	0	3
9.	POE2416	Ethical Management	3	0	0	3
10.	POE2417	Integrated Water Resources Management	3	0	0	3
11.	POE2418	Water, Sanitation and Health	3	0	0	3
12.	POE2420	Block chain Technologies	3	0	0	3
13.	POE2423	Energy Conservation and Management in Domestic Sectors	3	0	0	3
14.	POE2424	Additive Manufacturing	3	0	0	3
15.	POE2425	Electric Vehicle Technology	3	0	0	3

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CREDITS SUMMARY

S.NO	CATEGORY	TOTAL CREDITS				PERCENTAGE	
		I	II	III	IV		
1.	FC	4				4	5.26
2.	PCC	16	15			31	40.79
3.	PEC	-	6	10		16	21.05
4.	RMC	2				2	2.63
5.	OEC			3		3	3.94
6.	EEC		1	7	12	20	26.32
7.	Non Credit/Audit Course	0	0			0	-
TOTAL		22	22	20	12	76	100%

For Students admitted from 2025 year onwards.

FC – Foundation Courses
PCC – Professional Core Courses
PEC – Professional Elective Courses
RMC – Research Methodology and IPR Courses
OEC – Open Elective Courses
EEC – Employment Enhancement Course

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PAMAET2411	APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS					
		Category	L	T	P	Credit
		FC	3	1	0	4
Course objectives						
	• To introduce the fundamentals of fuzzy logic. • To understand the basics of random variables with emphasis on the standard discrete and continuous distributions. • To understand the basic probability concepts with respect to two dimensional random variables. • To make students understand the notion of a Markov chain, and how simple ideas of conditional probability and matrices can be used to give a thorough and effective account of discrete – time Markov chains. • To provide the required fundamental concepts in queueing models and apply these techniques in networks, image processing.					
UNIT – I	**FUZZY LOGIC**					**12**
Classical logic–Multi valued logics–Fuzzy propositions–Fuzzy qualifiers.						
UNIT – II	**PROBABILITY AND RANDOM VARIABLES**					**12**
Probability–Axioms of probability–Conditional probability–Bayes theorem–Random variables–Probability function – Moments – Moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a random variable.						
UNIT – III	**TWO DIMENSIONAL RANDOM VARIABLES**					**12**
Joint distributions – Marginal and conditional distributions – Functions of two dimensional random variables – Regression curve – Correlation.						
UNIT – IV	**RANDOM PROCESSES**					**12**
Classification – Stationary random process – Markov process – Markov chain – Poisson process – Gaussian process - Auto correlation – Cross correlation.						
UNIT – V	**QUEUEING MODELS**					**12**
Poisson process – Markovian queues – Single and multi server models – Little's formula –Machine Interference model – Steady state analysis – Self service queue.						
						Total: 60 periods

TEXT BOOK:

1. Essential of applied mathematics for scientist and Engineers by Robert G.Watts

REFERENCES:

1. Ganesh M., "Introduction to Fuzzy Sets and Systems, Theory and Applications", AcademicPress, New York, 1997.
2. GeorgeJ. Klir andYuanB," Fuzzy setsandFuzzy logic" PrenticeHall
3. Devore J.L, "Probability and Statistics for Engineering and Sciences", Cengage learning, 9th

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	Edition, Boston, 2017.
4.	Johnson R.A. and Gupta, C.B., " Miller and Freunds Probability and Statistics for Engineers", Pearson India Education, Asia, 9th Edition, New Delhi, 2017.
5.	Oliver C. Ibe," Fundamentals of applied probability and Random process", Academic press, Boston, 2014.
6.	GrossD.andHarris C.M.,"FundamentalsofQueuingtheory", Willeystudent, 3rd Edition, New Jersey, 2004.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Applythe concepts of fuzzysets,fuzzylogic, fuzzyprepositions andfuzzy quantifiersand in relate.	K3
CO2:	Analyze the performance interms of probabilities and distributions achieved by the determined solutions	K4
CO3:	Use some of the commonly encountered two dimensional random variables andextendto multivariate analysis.	K2
CO4:	Classifyvariousrandomprocessesandsolveproblemsinvolvingtochasticprocesses.	K2
CO5:	Use queueing models to solve practical problems.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	2	-	-	-
CO2	1	-	2	-	-	-
CO3	-	-	-	2	1	-
CO4	-	-	-	2	-	-
CO5	-	-	-	-	2	2
Avg.	2	-	2	2	2	2

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PRMT2411	RESEARCH METHODOLOGYAND IPR					
		Category	L	T	P	Credit
		RMC	2	0	0	2
Course objectives						
	• To give an overview of the research methodology and explain the technique of defining a research problem • To explain carrying out a literature search, its review, developing theoretical and conceptual frameworks and writing are view. • To explain the art of interpretation and the art of writing research reports. • To explain various forms of the intellectual property, its relevance and business impact in the changing global business environment. • To discuss leading International Instruments concerning Intellectual Property Rights.					
UNIT – I	**RESEARCH DESIGN**					**6**
Overview of research process and design,Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.						
UNIT – II	**DATA COLLECTION AND SOURCES**					**6**
Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods. Data - Preparing, Exploring, examining and displaying.						
UNIT – III	**DATA ANALYSIS AND REPORTING**					**6**
Overview of Multivariate analysis, Hypotheses testing and Measures of Association. Presenting Insights and findings using written reports and oral presentation						
UNIT – IV	**INTELLECTUAL PROPERTY RIGHTS**					**6**
Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.						
UNIT – V	**PATENTS**					**6**
Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licenses, Licensing of related patents, patent agents, Registration of patent agents.						
						Total: 30 periods
TEXT BOOK:						
1.	Research Methodology: Methods and Techniques C.R.Kothari, Gaurav Garg New Age International 4th Edition,2018.					

2.	Research Methodology a step-by-step guide for beginners.(For the topic Reviewing the literature under module 2)

REFERENCES:

1.	Cooper Donald R,Schindler Pamela Sand SharmaJK,"Business Research Methods", Tata McGraw Hill Education, 11e (2012).
2.	Catherine J.Holland,"Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets", Entrepreneur Press, 2007.
3.	David Hunt, Long Nguyen, Matthew Rodgers, "Patent searching: tools & techniques",Wiley, 2007.
4.	The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Discuss research methodology and the technique of defining a research problem	K2
CO2:	Explain the functions of the literature review in research, carrying out a theoretical and conceptual frameworks and writing a review.	K2
CO3:	Explain various research designs and their characteristics.	K2
CO4:	Explain the art of interpretation and the art of writing research reports.	K2
CO5:	Explain about the features and uses of patents.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	2	-	-	-
CO2	1	-	2	-	-	-
CO3	-	-	-	2	1	-
CO4	-	-	-	2	-	-
CO5	-	-	-	-	2	2
Avg.	2	-	2	2	2	2

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPT2401	ADVANCED DIGITAL SIGNAL PROCESSING					
		Category	L	T	P	Credit
		PCC	3	0	0	3
Course objectives						
	• To describe fundamental concepts of DSP and Discrete Transforms • To design digital filters design • To estimate power spectrum using non-parametric and parametric methods • To analyze the Multirate Signal processing by decimation and interpolation. • To apply the concept of multirate signal processing for various applications					
UNIT – I	**DIGITAL SIGNAL PROCESSING**					**9**
Sampling of analog signals - Selection of sampling frequency - Frequency response - Transfer functions - Filter structures - Fast Fourier Transform (FFT) Algorithms - Image coding - DCT						
UNIT – II	**DIGITAL FILTER DESIGN**					**9**
IIR and FIR Filters: Filter structures, Implementation of Digital Filters - 2nd Order Narrow Band Filter and 1st Order All Pass Filter, Frequency sampling structures of FIR, Lattice structures, Forward and Backward prediction error filters, Reflection coefficients for lattice realization, Implementation of lattice structures for IIR filters, Advantages of lattice structures.						
UNIT – III	**ESTIMATION OF POWER SPECTRUM**					**9**
Non-Parametric Methods: Estimation of spectra from finite duration observation of signals, Bartlett, Welch & Blackman- Tukey methods, Performance Comparison. Parametric Methods: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation						
UNIT – IV	**MULTIRATE SIGNAL PROCESSING**					**9**
Decimation by a factor D - Interpolation by a factor I - Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design and Implementation for sampling rate conversion. Up-sampling using All Pass Filter.						
UNIT – V	**APPLICATIONS OF MULTI RATE SIGNAL PROCESSING AND DSP INTEGRATED CIRCUITS**					**9**
Design of Phase Shifters, Interfacing of Digital Systems with Different Sampling Rates, Implementation of Narrow Band Low Pass Filters, Implementation of Digital Filter Banks, Sub band Coding of Speech Signals, Quadrature Mirror Filters, Over Sampling A/D and D/A Conversion.						
						Total: 45 periods
TEXT BOOK:						
1.	S.K. Mitra: Digital Signal Processing: A Computer-Based Approach, McGraw Hill Higher Education,2006,3rd edition					
REFERENCES:						
1.	J. G. Proakis, D. G. Manolakis: Digital Signal Processing: Principles, Algorithms, and					

	Applications, Prentice Hall, 2007, 4th edition
2.	AlanVOppenheim&RonaldWschafferDiscreteTimesignalprocessing,Pearson Education, 2014.
3.	KeshabK.Parhi,'VLSI Digital Signal Processing Systems Design and Implementation", John Wiley& Sons, 2007.
4.	Steven.M.Kay,Modern Spectral Estimation:Theory&Application–PHI,2009.
5.	P.Vaidyanathan,Multirate Systems and Filter Banks,Pearson Education,1993.
6.	Emmanuel C.Ifeachor, BarrieW.Jervis, "Digital Signal Processing–Apractical approach", Second Edition, Harlow, Prentice Hall, 2011.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Describe the basics of Digital Signal Processing and Discrete Time Transforms.	K2
CO2:	Design and implement FIR/IIR digital filters using various structures	K2
CO3:	Estimate power spectrum using appropriate parametric/ non-parametric method	K2
CO4:	Analyze discrete time system at different sampling frequencies using the concept of Multirate signal processing	K4
CO5:	Design discrete time system for the given application using Multirate signal processing.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	3	2	-	-
CO2	-	-	3	3	-	-
CO3	-	-	2	3	-	-
CO4	-	-	-	2	2	-
CO5	-	-	2	-	2	-
Avg.	-	-	3	3	2	-

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPT2402	ADVANCED DIGITAL SYSTEM DESIGN					
		Category	L	T	P	Credit
		PCC	3	0	2	4
Course objectives						
	• To design asynchronous sequential circuits. • To learn about hazards in asynchronous sequential circuits. • To study the fault testing procedure for digital circuits. • To understand the architecture of programmable devices. • To design and implement digital circuits using programming tools.					
UNIT – I	**SEQUENTIAL CIRCUIT DESIGN**					**9**
Analysis of Clocked Synchronous Sequential Circuits and Modelling- State Diagram, State Table, State Table Assignment and Reduction-Design of Synchronous Sequential Circuits Design of Iterative Circuits-ASM Chart and Realization using ASM.						
UNIT – II	**ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN**					**9**
Analysis of Asynchronous Sequential Circuit – Flow Table Reduction-Races-State AssignmentTransition Table and Problems in Transition Table- Design of Asynchronous Sequential Circuit - Static, Dynamic and Essential hazards – Mixed Operating Mode Asynchronous Circuits – Designing Vending Machine Controller.						
UNIT – III	**FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS**					**9**
Fault Table Method-Path Sensitization Method – Boolean Difference Method - D Algorithm — Tolerance Techniques – The Compact Algorithm – Fault in PLA – Test Generation - DFT Schemes – Built in Self Test.						
UNIT – IV	**SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES**					**9**
Programming Logic Device Families – Designing a Synchronous Sequential Circuit using PLA/PAL – Designing ROM with PLA – Realization of Finite State Machine using PLD – FPGA – Xilinx FPGA - Xilinx 4000.						
UNIT – V	**SYSTEM DESIGN USING VERILOG**					**9**
Hardware Modelling with Verilog HDL – Logic System, Data Types And Operators For Modelling In Verilog HDL - Behavioural Descriptions In Verilog HDL – HDL Based Synthesis – Synthesis Of Finite State Machines– Structural Modelling – Compilation And Simulation Of Verilog Code – Test Bench - Realization Of Combinational And Sequential Circuits Using Verilog – Registers – Counters – Sequential Machine – Serial Adder – Multiplier- Divider – Design Of Simple Microprocessor, Introduction To System Verilog.						
						Total: 45 periods
PRACTICAL EXERCISES:						**30 PERIODS**
1. Design of Registers by Verilog HDL.						
2. Design of Counters by Verilog HDL.						
3. Design of Sequential Machines by Verilog HDL.						

4. Design of Serial Adders , Multiplier and Divider by Verilog HDL.	
5. Design of a simple Microprocessor by Verilog HDL.	
	Total: 75 periods
TEXT BOOK:	
1.	Shirshendu Roy- Advanced Digital System Design: A Practical Guide to Verilog Based FPGA and ASIC Implementation- Wiley / Self-published 2023.
2.	Michael D. Ciletti- Advanced Digital Design with the Verilog HDL, Pearson Education 2010
3.	Charles H. Roth Jr. & Larry L. Kinney, Fundamentals of Logic Design, Cengage Learning 2014
REFERENCES:	
1.	Charles H.Roth jr., "Fundamentals of Logic Design" Thomson Learning,2013.
2.	M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3.	M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4.	Nripendra N Biswas "Logic Design Theory" Prentice Hall of India,2001.
5.	Paragk.Lala "Fault Tolerant and Fault Testable Hardware Design" B S Publications,2002
6.	Paragk.Lala "Digital System Design Using PLD" B S Publications,2003.
7.	Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Analyse and design synchronous sequential circuits.	K2
CO2:	Analyse hazards and design asynchronous sequential circuits.	K2
CO3:	Knowledge on the testing procedure for combinational circuit and PLA.	K2
CO4:	Able to design PLD and ROM.	K4
CO5:	Design and use programming tools for implementing digital circuits of industry standards.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	-	1	-	1
CO2	-	-	1	2	-	1
CO3	-	-	1	2	1	-
CO4	-	-	1	2	2	-
CO5	-	-	1	2	-	-
Avg.	-	-	1	2	1	1

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPT2403	SEMICONDUCTOR DEVICES AND MODELING					
		Category	L	T	P	Credit
		PCC	3	0	0	3
Course objectives						
	• To acquire the fundamental knowledge and to expose to the field of semiconductor theory and devices and their applications. • To gain adequate understanding of semiconductor device modelling aspects, designing devices for electronic applications • To acquire the fundamental knowledge of different semiconductor device modelling aspects.					
UNIT – I	**MOS CAPACITORS**					**9**
Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Non equilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown.						
UNIT – II	**MOSFET DEVICES**					**9**
Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Sub threshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields						
UNIT – III	**CMOS DEVICE DESIGN**					**9**
CMOS Scaling, Constant-Field Scaling, Generalized Scaling, Non scaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Non uniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, 16 Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements.						
UNIT – IV	**BIPOLAR DEVICES**					**9**
n–p–n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Non ideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages,						

Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor.		
UNIT – V	**MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS**	**9**
Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.		
		Total: 45 periods

TEXT BOOK:	
1.	Yuan Taur & Tak H. Ning, Fundamentals of Modern VLSI Devices "Cambridge University Press", 2022
2.	A. B. Bhattacharyya, Compact MOSFET Models for VLSI Design "Wiley", 2009
3.	Trond Ytterdal, Yuhua Cheng & Tor A. Fjeldly, Device Modeling for Analog and RF CMOS Circuit Design, "Wiley", 2004
REFERENCES:	
1.	Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.
2.	A.B. Bhattacharyya "Compact MOSFET Models for VLSI Design", John Wiley & Sons Ltd, 2009.
3.	Ansgar Jungel, "Transport Equations for Semiconductors", Springer, 2009
4.	Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd, 2004
5.	Selberherr, S., "Analysis and Simulation of Semiconductor Devices", Springer-Verlag., 1984
6.	Behzad Razavi, "Fundamentals of Microelectronics" Wiley Student Edition, 2nd Edition, 2014
7.	J P Collinge, C A Collinge, "Physics of Semiconductor devices" Springer, 2002.
8.	S.M.Sze, Kwok.K. NG, "Physics of Semiconductor devices", Springer, 2006.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Explore the properties of MOS capacitors.	K2
CO2:	Analyze the various characteristics of MOSFET devices.	K2
CO3:	Describe the various CMOS design parameters and their impact on performance of the device.	K2
CO4:	Discuss the device level characteristics of BJT transistors.	K4
CO5:	Identify the suitable mathematical technique for simulation.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	2	2	3
CO2	-	-	1	3	-	2
CO3	3	-	3	3	1	2
CO4	-	-	2	3	3	3
CO5	-	-	1	3	1	2

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Avg.	3	-	2	3	1	2
1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy						

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PAPT2404	DIGITAL CMOS VLSI DESIGN					
		Category	L	T	P	Credit
		PCC	3	0	0	3
Course objectives						
	• To introduce the transistor level design of all digital building blocks common to all cmos microprocessors, network processors, digital backend of all wireless systems etc. • To introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures • To learn all important issues related to size, speed and power consumption					
UNIT – I	**MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER**					**12**
MOSFET characteristic under static and dynamic conditions, MOSFET secondary effects, elmore constant , CMOS inverter-static characteristic, dynamic characteristic, power, energy, and energy delay parameters, stick diagram and layout diagrams.						
UNIT – II	**COMBINATIONAL LOGIC CIRCUITS**					**9**
Static CMOS design, different styles of logic circuits, logical effort of complex gates, static and dynamic properties of complex gates, interconnect delay, dynamic logic gates.						
UNIT – III	**SEQUENTIAL LOGIC CIRCUITS**					**9**
Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, nonbistable sequential circuits.						
UNIT – IV	**ARITHMETIC BUILDING BLOCKS**					**9**
Data path circuits, architectures for adders, accumulators, multipliers, barrel shifters, speed, power and area tradeoffs.						
UNIT – V	**MEMORY ARCHITECTURES**					**6**
Memory architectures and Memory control circuits: Read-Only Memories, ROM cells, ReadWrite Memories (RAM), dynamic memory design, 6 Transistor SRAM cell, sense amplifiers.						
Total: 45 periods						
TEXT BOOK:						
1.	Neil H. E. Weste and David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Pearson Education 4th Ed., 2015					
2.	Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, Pearson Education 2nd Ed., 2003.					
REFERENCES:						
1.	N.Weste, K. Eshraghian, " Principles Of Cmos VLSI Design", Addision Wesley, 2nd Edition, 1993					
2.	M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997					
3.	Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis And Design", Mcgraw-Hill, 1998					

4.	Jan Rabaey, Anantha Chandrakasan, B Nikolic, " Digital Integrated Circuits: A Design Perspective", Prentice Hall Of India, 2nd Edition, Feb 2003

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Use mathematical methods and circuit analysis models in analysis of CMOS digital circuits	K2
CO2:	Create models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort	K2
CO3:	Design sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches	K2
CO4:	Understand design methodology of arithmetic building blocks	K4
CO5:	Design functional units including ROM and SRAM	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	-	2	-	-	-
CO2	-	-	3	2	-	-
CO3	-	-	3	3	-	-
CO4	-	-	-	1	2	2
CO5	-	-	-	2	-	2
Avg.	1	-	3	2	2	2

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPL2401	ELECTRONICS SYSTEM DESIGN LABORATORY

Category	L	T	P	Credit
PCC	0	0	3	1.5

Course objectives

- Design of instrumentation amplifier and voltage regulator
- Design of PCB layout
- Write a Verilog HDL coding of various combinational circuits
- Verify the design functionality for various memory modules
- Design of PLL circuits

LIST OF EXPERIMENTS:

1. Design of a 4-20m A transmitter for a bridge type transducer.
   Design the Instrumentation amplifier with the bridge type transducer (Thermistor or any resistance variation transducers) and convert the amplified voltage from the instrumentation amplifier to 4 – 20 mA current using op-amp. Plot the variation of the temperature Vs output current.

2. Design of AC/Dc voltage regulator using SCR
   Design a phase controlled voltage regulator using full wave rectifier and SCR, vary the conduction angle and plot the output voltage.

3. PCB layout design using CAD
   Drawing the schematic of simple electronic circuit and design of PCB layout using CAD

4. HDL based design entry and simulation of Parameterizable cores of Counters, Shift registers, State machines, 8-bit Parallel adders and 8 –Bit multipliers.

5. HDL based design entry and simulation of Parameterizable cores on the simple Distributed Arithmetic system. Test vector generation and timing analysis.

6. HDL based design entry and simulation of Parameterizable cores on memory design and 4 –bit ALU. Synthesis, P&R and post P&R simulation, Critical paths and static timing analysis results to be identified. FPGA real time programming and I/O interfacing.

7. Interfacing with Memory modules in FPGA Boards. Verifying design functionality by probing internal signals.

8. Invoke PLL module and demonstrate the use of the PLL for clock generation in FPGAs. Verify design functionality implemented in FPGA by capturing the signal in Oscilloscope.

PAPL2402	SIGNAL PROCESSING LABORATORY

Category	L	T	P	Credit
PCC	0	0	3	1.5

Course objectives

- To provide the student with the basic understanding of audio signal analysis using filters
- To provide the students with the understanding of the working of statistical method based approaches
- To impart the students with the design of filters
- To demonstrate the working of algorithms for different applications
- To provide knowledge of analyzing the images and video

LISTOF EXPERIMENTS

1. Design of Adaptive channel equalizer
2. Realization of subb and filter using linear convolution
3. Realization of STFT using FFT
4. Demonstration of Bayes technique
5. Demonstration of Min-max technique
6. Realization of FIR Wiener filter
7. Generation of Multi variate Gaussian generated data with desired mean vector and the required co-variance matrix.
8. Design and Realization of the adaptive filter using LMS algorithm (solve dusing steepest- descent algorithm)
9. Representation of the 2D image signal as the linear combinations of PCA (Eigen faces)
10. Image compression using Discrete cosine transformation(DCT).
11. Multiple-input Multiple output (MIMO)
12. Speech recognition using Support Vector Machine(SVM)
13. LMS filtering implementation using TMS320C6x processor
14. Face detection and tracking in video using Open CV

TOTAL:45 PERIODS

COURSE OUTCOMES:

CO1: Obtain the ability to apply knowledge of linear algebra ,random process and multirate signal processing in various signal processing applications.

CO2: Develop the student's ability on conducting engineering experiments ,analyze experimental observations scientifically

CO3: Become familiar to fundamental principles of linear algebra

CO4: Familiarize the basic operations of filter banks through simulations

CO5: Apply the principles of random process in practical applications

PAPT2421	ANALOG AND MIXED SIGNAL IC DESIGN					
		Category	L	T	P	Credit
		PCC	3	0	0	3
Course objectives						
	• To study the concepts of MOS large signal model and small signal model • To provide in-depth understanding of the analog integrated circuit and building blocks • To learn the Analog and Digital layout design for mixed signal circuits • To Understand the methodologies for analysis and design of fundamental CMOS Analog and Mixed signal Circuits like Data Converters and filters. • To study the integrated circuits like oscillators and PLLs.					
UNIT – I	**INTRODUCTION AND BASIC MOS DEVICES**					**9**
Challenges in analog design-Mixed signal layout issues-MOSFET structures and characteristics-large signal model–small signal model-single stageAmplifier-Source follower- Common gate stage – Cascode Stage						
UNIT – II	**SUB MICRON CIRCUIT DESIGN**					**9**
Submicron CMOS process flow, Capacitors and resistors, Current mirrors, The MOSFET Switch, Analog Circuit Design: Biasing, Op-Amp Design, Circuit Noise -OP Amp parameters						
UNIT – III	**DATA CONVERTERS**					**9**
Characteristics of Sample and Hold-Digital to Analog Converters-architecture-Differential Non linearity-Integral Nonlinearity-Voltage Scaling-Cyclic DAC-Pipeline DAC-Analog to Digital Converters-architecture–Flash ADC-Pipeline ADC-Differential Nonlinearity-Integral Nonlinearity.						
Overview of SNR of Data Converters-ClockJitters-Improving Using Averaging–Decimating Filters for ADC- Band pass and High Pass Sinc Filters- Interpolating Filters for DAC						
UNIT – IV	**ANALOG AND DIGITAL LAYOUT DESIGN FOR MIXED SIGNAL**					**9**
Layout introduction: Introduction, MOS transistor layers, stick diagram, symbolic diagram. Digital layout design: Introduction, guide line of transistor layout, PMOS and NMOS transistor layout, CMOS transistor layout. Introduction toanalog layout techniques and Passive component layout - capacitor, resistor and inductor, Floor planning of analog and digital components, power supplyand ground pin issues, matching, shielding, interconnection issues.						
UNIT – V	**OSCILLATORS AND PLL**					**9**
LC oscillators, Voltage Controlled Oscillators. Simple PLL, Charge pumps PLLs, Non ideal effects in PLLs, Delay Locked Loops. Applications of PLL.frequency multiplication and synthesis. Introduction to RF IC Design, building blocks, applications						
						Total: 45 periods
REFERENCES:						

1.	P.Allen and D.Holberg,"CMOS Analog Circuit Design",Oxford University Press,Second Edition, 2012.
2.	B.Razavi,"Design of Analog CMOS Integrated Circuits",Mc GrawHill,2003.
3.	R.Jacob Baker,H.W.Li,andD.E.Boyce CMOS Circuit Design,Layout and Simulation, Prentice-Hall of India,1998.
4.	PaulR.Gray,PaulJ.Hurst,Stephen H.Lewis,RobertG.Meyer,"Analysis and Design of Analog Integrated Circuits", Wiley Publishers, Fifth Edition, 2009.

COURSE OUTCOMES: At the end of this course the students will be able to:		**BT Mapped (Highest Level)**
CO1:	Carry out research and development in the area of analog and mixed signal IC design.	K2
CO2:	Well versed with the MOS fundamentals, small signal models and analysis of MOSFET based circuits.	K2
CO3:	Analyse and model data converters architecture	K2
CO4:	Understand and Design different mixed signal circuits for various applications as per the user specifications.	K2
CO5:	Analyze and design mixed signal circuits such as Comparator ,ADCs,DACs,PLL.	K4

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	-	-	-	-
CO2	-	-	3	1	-	-
CO3	-	-	2	2	-	-
CO4	-	-	-	2	2	-
CO5	-	-	-	2	-	-
Avg.	3	-	3	2	2	2

PAPT2422	INDUSTRIAL INTERNET OF THINGS	

Category	L	T	P	Credit
PCC	3	0	0	3

Course objectives	
	• To understand the fundamentals of Internet of Things • To learn about the basics of IOT protocols • To build a small low cost embedded system using IoT • To apply the concept of IoT in the real world scenario

UNIT – I	INTRODUCTION AND ARCHITECTURE OF IoT	9

Introduction – Definition and characteristics of IoT – Physical and Logical Design of IoT - Communication models and APIs – Challenges in IoT - Evolution of IoT- Components of IoT - A Simplified IoT Architecture – Core IoT Functional Stack.

UNIT – II	INDUSTRIAL IoT	9

IIoT-Introduction, Industrial IoT: Business Model and Reference Architecture: IIoT-Business Models, Industrial IoT- Layers: IIoT Sensing, IIoT Processing, IIoT Communication, IIoTNetworking

UNIT – III	IIOT ANALYTICS	9

Big Data Analytics and Software Defined Networks, Machine Learning and Data Science, Julia Programming, Data Management with Hadoop

UNIT – IV	IOT SECURITY	9

Industrial IoT: Security and Fog Computing - Cloud Computing in IIoT, Fog Computing in IIoT, Security in IIoT

UNIT – V	CASE STUDY	9

Industrial IOT- Application Domains: Oil, chemical and pharmaceutical industry, Applications of UAVs in Industries, Real case studies: Milk Processing and Packaging Industries, Manufacturing Industries

Total: 45 periods

REFERENCES:

1. Industry 4.0:The Industrial Internet of Things",by Alas dair Gilchrist (Apress),2017
2. "Industrial Internet of Things:Cyber manufacturing Systems"by Sabina Jeschke, Christian Brecher, Houbing Song, Danda B. Rawat (Springer), 2017
3. Hands-On Industrial Internet of Things:Create a powerful Industrial IoT by Giacomo Veneri,

	Antonio Capasso, Packt, 2018.

COURSE OUTCOMES: Upon completion of this course,student will be able to		**BT Mapped (Highest Level)**
CO1:	Understand the basic concepts and Architectures of Internet of Things.	K2
CO2:	Understand various IoT Layers and the irrelative importance.	K2
CO3:	Realize the importance of Data Analytics in IoT.	K2
CO4:	Study various IoT platforms and Security	K2
CO5:	Understand the concepts of Design Thinking.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	1	-	-
CO2	-	-	2	1	-	-
CO3	-	-	3	2	-	-
CO4	-	-	-	-	2	-
CO5	-	-	-	-	1	1
Avg.	-	-	2	1	2	1

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PAPT2423	POWER CONVERSION CIRCUITS FOR ELECTRONICS					
		Category	L	T	P	Credit
		PCC	3	0	0	3
Course objectives						
	• To provide the students a deep insight into the working of different switching devices with respect to their characteristics • To analyze different converters with their applications. • To study advanced converters and switching techniques implemented in recent technology					
UNIT – I	**POWER ELECTRONIC DEVICES AND SEMICONDUCTOR SWITCHES**					**9**
Introduction, Applications of power electronics, Power electronics devices: Characteristics of power devices – characteristics of SCR, diac, triac, GTO, PUJT, power transistors – power FETs – L ASCR – two transistor model of SCR Protection of thyristors against over voltage – over current, dv/dt and di/dt. Power Semiconductor Switches: Rectifier diodes, fast recovery diodes.						
UNIT – II	**SCR PERFORMANCE AND APPLICATIONS**					**9**
Turn oncircuitsfor SCR – triggering with single pulse and train of pulses synchronizing with supply – Thyristor turn off methods, natural and forced commutation, self-commutation series and parallel operations of SCRs. Rectifiers: Single phase and three phase controlled Rectifiers with inductive loads, RL load. Construction & Workingof Opto- Isolators, Opto-TRIAC, Opto-SCR.						
UNIT – III	**INVERTERS AND VOLTAGE CONTROLLERS**					**9**
Voltage and current source inverters, resonant, Series inverter, PWM inverter. AC and DC choppers – DC to DC converters – Buck, boost and buck – boost. Single phase and three phase Cyclo- conveters, Power factor control and Matrix Converters. Industrial applications DC and AC Drives DC Motor Speed control Induction Motor Speed Control						
UNIT – IV	**TIMERS& DELAY ELEMENTS,HIGH FREQUENCY POWER HEATING, SENSOR AND ACTUATORS**					**9**
RC Base Constant Timers, Timer Circuits using SCR, IC-555, Programmable Timer and their Industrial Applications, Induction Heating and Dielectric Heating System and Their Applications, Sensors, Transducers, and Transmitters for Measurement, Control & Monitoring : Thermoresistive Transducer, Photoconductive Transducers, Pressure Transducers, Flow Transducers, Level Sensors, Speed Sensing, Vibration Transducers, Variable-Frequency Drives, Stepper Motors and Servomotor Drives.						
UNIT – V	**AUTOMATION AND CONTROL**					**9**
Data Communications for Industrial Electronics, Telemetry, SCADA & Automation, AC & DC Drives, Voltage & Power Factor Control through Solid State Devices, Soft Switching, Industrial Robots.						
						Total: 45 periods
REFERENCES:						

1.	Thomas E. Kissell, Industrial Electronics: Applications for Programmable Controllers, Instrumentation and Process Control, and Electrical Machines and Motor Controls, 3rd edition, 2003, Prentice Hall
2.	B.Paul,Industrial Electronic and Control,Prentice Hall of India Private Limited (2004).
3.	M.H. Rashid, "Power Electronics: Circuits, Devices & Applications", Prentice Hall of IndiaLtd. 3rd Edition, 2004.
4.	G.K.Dubey, Power Semiconductor Controlled Drives, Prentice Hall inc.(1989).

COURSE OUTCOMES:		**BT Mapped (Highest Level)**
CO1:	Describe the characteristics, operation of power switching devices and identify their ratings and applications	K2
CO2:	Understand the requirements SCR Protection, Describe the Functioning of SCR their Construction and Performance.	K2
CO3:	Analyze and Design the Converter Based on SCR for various Industrial Applications.	K4
CO4:	Demonstrate ability to understand High Frequency, Heating Systems, Timers, Relevant Sensors & Actuator and their Application in Industrial Setting.	K2
CO5:	Demonstrate the ability to understand and apply Data Communication, Telemetry &SCADA System in Industrial Applications.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	2	-	-	-
CO2	1	-	2	-	-	-
CO3	-	-	-	2	1	-
CO4	-	-	-	2	-	-
CO5	-	-	-	-	2	2
Avg.	2	-	2	2	2	2

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPT2424	EMBEDDED SYSTEMS				
	Category	L	T	P	Credit
	PCC	3	0	2	4
Course objectives					
	• Learn Embedded design challenges and design methodologies • Study general and single purpose processor • Understand bus structures • Design a state machine and concurrent process models • Know about Embedded software development tools and RTOS				
UNIT – I	**EMBEDDED SYSTEM OVERVIEW**				**9**
Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single- Purpose Processors.					
UNIT – II	**GENERAL AND SINGLE PURPOSE PROCESSOR**				**9**
Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer's view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to- Digital Converters, Memory Concepts.					
UNIT – III	**BUS STRUCTURES**				**9**
Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11.					
UNIT – IV	**STATE MACHINE AND CON CURRENT PROCESS MODELS**				**9**
Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems,Automation:Synthesis,Verification:Hardware/SoftwareCo-Simulation,Reuse: Intellectual Property Cores, Design Process Models					
UNIT – V	**EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS**				**9**
Compilation Process–Libraries–Porting kernels–C extensions for embedded systems–emulation and debugging techniques – RTOS – System design using RTOS.					

PRACTICAL LIST:

Exercise–1

Comparative study of software development tools and design steps with respect to FPGA based and Non – FPGA based (defined logic) embedded system development.

(For Example: consider any Spartan FPGA board for FPGA based Embedded System Consider any cortex-M based board for Non – FPGA based Embedded system)

Exercise–2

Implement adder and decoder logic blocks in any one of the FPGA chip baseddevelopment board.

Exercise–3

Design and development of UART protocol logic block in any one of FPGA chip based development

board.

Exercise–4

Consider on board LEDS (any four) and timer logic block of cortex- M board.Write a program which enables LEDS to glow in different timing.

Exercise–5

Consider on board switches and (2x16) LCD display develop a program which displays the status of switch activation.

Exercise–6

Demonstrate GPIO based I/O interfacing by considering LM 35 temperature sensor and cortex- M board.

Exercise–7

Development of one interfacing scheme which transmits data from one cortex- M board to another cortex- M board using on chip CAN logic blocks.

Exercise–8

Consider on board EPROM IC of Cortex- M board by utilizing on chip I2c logic block transmitdata to EPROM ICand receive stored data from EPROM IC.

Total: 75 periods

REFERENCES:

1. Powel Douglas, "Realtime UML, second edition: Developing efficient objects for embedded systems", 3rd Edition 1999, Pearson Education.
2. Daniel W.Lewis, "Fundamentals of embedded software where C and assembly meet", Pearson Education, 2002.
3. Frank Vahidand Tony Gwargie, "Embedded System Design", John Wiley&sons,2002.
4. SteveHeath,"EmbeddedSystemDesign",Elsevier,SecondEdition,2004

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Able to design an Embedded system	K2
CO2:	Understand a general and single purpose processor	K2
CO3:	Explain different protocols	K2
CO4:	Discuss state machine and design process models	K2
CO5:	Outline embedded software development tools and RTOS	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	-	-	-	-
CO2	-	-	2	1	-	-
CO3	-	-	-	1	2	-
CO4	-	-	2	-	1	-
CO5	-	-	-	-	2	1
Avg.	2	-	2	1	2	1

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPL2421	VLSI DESIGN LABORATORY

Category	L	T	P	Credit
PCC	0	0	4	2

Course objectives

- Familiarize with different FPGA boards
- Analyze digital design using Front end Tools
- Analyze the CMOS circuits using CAD tools
- Analyze the interfacing of I/O devices with Arduino Boards using Embedded C

PRACTICALEXPERIMENTS:

1. Synthesize and implement Combinational and Sequential Circuits in VERILOG/VHDL
2. Synthesize and implement MAC unit and GCD unit in Verilog/VHDL
3. Implementation of sampling of input signal and display in FPGA Synthesize and implement FIR filter and IIR filter Verilog /VHDL
4. Synthesize and implement 8bit general purpose processor inVerilog/VHDL
5. Synthesize and implement UART and USART
   Simulation and Analysis of CMOS [illegible] using CAD tool

Total: 60 periods

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Program in Verilog/VHDL for combinational and sequential circuits and implement the program in FPGA	K2
CO2:	Implement FIR and IIR filters in FPGA	K2
CO3:	Implement data path design and interfaces	K2
CO4:	Handle CAD tools to draw/edit, and analyze the CMOS circuits	K2
CO5:	Program and interface the Arduino Boards using Embedded C	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6								
CO1	1	-	-	-	3	-								
CO2	2	-	-	-	2	-								
CO3	-	-	-	2	1	-								
CO4	2	-	-	2	-	-								
CO5	-	-	-	2	1	2								
Avg.	2	-	-	2	2	2								

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom`s Taxonomy

PAPL2422	MINI PROJECT WITH SEMINAR					
		Category	L	T	P	Credit
		EEC	0	0	2	1
Course objectives						
	• Understand and apply the methodology of selecting a relevant mini-project topic through literature review or need analysis. • Plan and design a technical solution, including selection of hardware/tools, defining architecture and methodology. • Demonstrate practical skills in building and implementing a working prototype based on the design. • Apply testing, debugging, data analysis, and iterative refinement techniques. • Develop effective communication skills through written reports and oral seminar delivery.					
UNIT – I	**PROJECT PROPOSAL & PLANNING**					**6**
Topic selection: conduct literature reviews & identify needs Define objectives, scope, deliverables, methodology, and timeline						
UNIT – II	**SYSTEM DESIGN & IMPLEMENTATION**					**6**
Design system architecture and select platforms/tools (e.g., microcontrollers, FPGA, sensors) Prototype development						
UNIT – III	**TESTING & PERFORMANCE EVALUATION**					**6**
Set up testing environments, perform data acquisition Debug and optimize designs						
UNIT – IV	**TECHNICAL SEMINAR**					**6**
Prepare a 15–20 min presentation with demonstration Engage in Q&A with faculty/peers						
UNIT – V	**FINAL REPORT & DOCUMENTATION**					**6**
Structure document (abstract, intro, methodology, results, conclusion, future scope) Reference accurately, incorporate feedback						
						Total: 30 periods

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Formulate and define an engineering problem through literature or need analysis.	K2
CO2:	Design a viable technical solution with system architecture and appropriate tools.	K2
CO3:	Implement and validate a prototype using core engineering principles.	K2
CO4:	Demonstrate effective teamwork and project management skills.	K4

CO5:	Communicate technical work through reports and oral presentations	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	-	-	-	-	-
CO2	1	1	-	-	-	-
CO3	-	1	1	-	-	-
CO4	-	-	-	1	-	-
CO5	-	-	-	-	1	1-
Avg.	1	-	1	1	1	1

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2401	APPLICATIONS SPECIFIC INTEGRATED CIRCUITS	

Category	L	T	P	Credit
PEC	3	0	0	3

Course objectives		
	• To prepare the student to be an entry-level industrial standard ASIC or FPGA designer • To analyze the issues and tools related to ASIC/FPGA design and implementation • To understand basics of System on Chip and Platform based design	
UNIT – I	**INTRODUCTION TO ASICS,CMOS LOGIC AND ASIC LIBRARY DESIGN**	**9**
Types of ASICs-Design flow-CMOS transistors-Combinational Logic Cell–Sequential logic cell -Data path logic cell-Transistors as Resistors-Transistor Parasitic Capacitance-Logical effort		
UNIT – II	**PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS**	**9**
Anti-fuse- static RAM- EPROM and EEPROM technology - Actel ACT – Xilinx LCA –Altera FLEX- Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks		
UNIT – III	**PROGRAMMABLE ASIC ARCHITECTURE**	**9**
Architecture and configuration of Spartan /Cyclone and Virtex / Stratix FPGAs–Micro-Blaze/ Nios based embedded systems – Signal probing techniques		
UNIT – IV	**LOGIC SYNTHESIS,PLACEMENT AND ROUTING**	**9**
Logic synthesis -ASIC floor planning-placement and routing–power and clocking strategies.		
UNIT – V	**HIGH PERFORMANCE ALGORITHMS FOR ASICs/SOCs. SOC CASE STUDIES**	**9**
DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators. Case Studies: Digital camera, SDRAM, High speed data standards		
		Total: 45 periods

REFERENCES:

1.	DouglasJ.Smith,HDLChipDesign,Madison,AL,USA:DoonePublications,1996
2.	Jose E. France, YannisTsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994
3.	M.J.S.Smith,"Application-SpecificIntegratedCircuits",Pearson,2003
4.	Mohammed Ismail andTerriFiez,"Analog VLSI Signal and Information Processing", McGraw Hill, 1994
5.	RogerWoods,JohnMcAllister,Dr.YingYi,GayeLightbod,"FPGA-basedImplementationof Signal Processing Systems", Wiley, 2008
6.	SteveKilts,"AdvancedFPGADesign,"WileyInter-Science,2007

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1:	To architect ASIC library design	K2
CO2:	To develop programmable ASIC logic cells	K2
CO3:	To design I/O cells and interconnects	K2
CO4:	To understand logic synthesis, placement and routing	K2
CO5:	To identify new developments in SOC and low power design	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	-	-	-	-
CO2	1	-	1	2	2	2
CO3	2	-	1	3	3	2
CO4	-	-	2	3	3	2
CO5	1	-	3	3	3	1
Avg.	1	-	2	3	3	2

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPE2402	COMPUTER ARCHITECTURE AND PARALLEL PROCESSING				
	Category	L	T	P	Credit
	PEC	3	0	0	3

Course objectives	
	• Discuss the basic concepts and structure of computers. • Explain the concepts of number representation and arithmetic operations. • Explain different types of Memory architectures. • Describe various parallel processing schemes and vector architecture. • Summarize the Instruction execution stages and Memory hierarchy

UNIT – I	INTRODUCTION TO COMPUTER ORGANIZATION	9

Architecture and function of general computer system - Basic Operational Concepts, Bus Structures, Software Performance – Memory locations & addresses – Memory operations – Instruction and instruction sequencing – addressing modes – assembly language - System buses, Multi-bus organization

UNIT – II	DATA REPRESENTATION	9

Signed number representation, fixed and floating point representations, character representation. Computer arithmetic - integer addition and subtraction, ripple carry adder, carry look-ahead adder - multiplication - shift-and-add, Booth multiplier, carry save multiplier - Division - non-restoring and restoring techniques, floating point arithmetic

UNIT – III	PROCESSOR ARCHITECTURE AND CONTROL UNIT	9

A Basic MIPS implementation – Building a Data path – Control Implementation Scheme – Hardwired control – micro programmed control - Pipelining – Pipelined data path and control – Handling Data Hazards & Control Hazards – Exceptions. Processor Architecture: Very Long Instruction Word (VLIW)Architecture, Digital Signal Processor Architecture, System on Chip (SoC) architecture, MIPS Processor and programming

UNIT – IV	PARALLEL PROCESSING	9

Parallel processing challenges – Flyn's classification – Single Instruction Single Data (SISD), Multiple Instruction Multiple Data (MIMD), Single Instruction Multiple Data (SIMD), Single Program Multiple Data (SPMD), and Vector Architectures-Hardware multithreading – Multi-core processors and other Shared Memory Multiprocessors - Introduction to Graphics Processing Units, Clusters, Warehouse Scale Computers and other Message-Passing Multiprocessors

UNIT – V	MEMORY & I/O SYSTEMS	9

Memory Hierarchy – memory technologies – cache memory – measuring and improving cache performance – virtual memory, Translation Look aside Buffers – Accessing I/O Devices – Interrupts – Direct Memory Access – Bus structure – Bus operation – Arbitration – Interface circuits – Universal Serial Bus.

Total: 45 periods

REFERENCES:

1. DavidA.PattersonandJohnL.Hennessy,"ComputerOrganizationandDesign:The Hardware/Software Interface", Morgan Kaufmann / Elsevier, 5th Edition, 2014
2. Carl Hamacher, Zvonko Vranesic, SafwatZaky and Naraig Manjikian, "Computer Organization

	and Embedded Systems", Tata McGraw Hill, 6th Edition, 2012.
3.	William Stallings,"ComputerOrganizationandArchitecture–DesigningforPerformance", Pearson Education, 8th Edition, 2010
4.	JohnP.Hayes,"ComputerArchitectureandOrganization",TataMcGrawHill,3rdEdition, 2012.
5.	John L. Hennessey and David A.Patterson, "Computer Architecture–A Quantitative Approach", Morgan Kaufmann / Elsevier Publishers, 5th Edition, 2012.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Understand the basic organization of computer and different instruction formats and addressing modes.	K2
CO2:	Interpret there presentation and manipulation of data on the computer.	K3
CO3:	Illustrate about implementation schemes of control unit and pipeline performance.	K2
CO4:	Summarize the various types of parallel is architectures.	K2
CO5:	Compare the various memory hierarchy and I/O systems.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	2	-	3
CO2	-	-	1	2	1	3
CO3	1	-	2	2	-	2
CO4	-	-	1	1	1	3
CO5	-	-	1	1	1	3
Avg.	1	-	1	2	1	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2403	AUTOMOTIVE ELECTRONICS					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• To explain the principle of electronic management system and different sensors used in the systems. • To know the concepts and develop basic skills necessary to diagnose automotive electronic problems. • To know Starting, and charging, lighting systems, advanced automotive electrical systems. • To include electronic accessories and basic computer control. • To explore practically about the components present in an Automotive electrical and electronics system.					
UNIT – I	**FUNDAMENTALS**					**9**
Components for electronic engine management system, open and closed loop control strategies, PID control, Look up tables, introduction to modern control strategies like Fuzzy logic and adaptive control. Switches, active resistors, Transistors, Current mirrors/amplifiers, Voltage and current references, Comparator, Multiplier. Amplifier, filters, A/D and D/A converters.						
UNIT – II	**MODERN SENSORS**					**9**
Film sensors, micro-scale sensors, Particle measuring systems, Vibration Sensors, SMART sensors, Machine Vision, Multi-sensor systems Applications of Sensors: Applications and case studies of Sensors in Automobile Engineering, Aeronautics, Machine tools and Manufacturing processes.						
UNIT – III	**CHARGING SYSTEM**					**9**
Generation of Direct Current- Shunt Generator Characteristics- Armature Reaction- Third Brush Regulation- Cutout. Voltage and Current Regulators- Compensated Voltage Regulator Alternators Principle and Constructional Aspects and Bridge Rectifiers- New Developments.						
UNIT – IV	**AUTOMOTIVE TRANSMISSION CONTROL SYSTEMS**					**9**
Transmission control - Cruise control – Braking control – Traction control –Suspension control – Steering control – Stability control – Integrated engine control.						
UNIT – V	**ELECTRONICS SYSTEMS**					**9**
Current Trends in Automotive Electronic Engine Management System- Types of EMS Electromagnetic interference Suppression- Electromagnetic Compatibility- Electronic Dashboard Instruments- Onboard Diagnostic System- Security - Warning System infotainment and Telematics.						
						Total: 45 periods
TEXT BOOK:						
1.	Bosch – Automotive Electrics and Automotive Electronics (5th ed., 2014)					
2.	William B. Ribbens – Understanding Automotive Electronics (6th ed., 2003)					
3.	Tom Denton – Automobile Electrical and Electronic Systems (4th ed., 2017)					
REFERENCES:						
1.	Allan Bonnick, "Automotive Computer Controlled Systems", Butterworth- Heinemann, Elsevier, Indian Edition, 2011.					

2.	Eric Chowanietz, "Automobile Electronics" by SAE Publications, 1995.
3.	Tom Weather Jr and Cland C. Hunter, "Automotive Computers and Control System" Prentice Hall Inc.,1984 New Jersey.
4.	R.K. Jurgen, "Automotive Electronics Handbook", McGraw Hill 2 nd Edition,1995.
5.	William B Ribbens, "understanding automotive electronics", 5th edition - Butter worth Heinemann Woburn, 1998.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Explain the fundamentals, operation, function of various sensors and actuators in engine management systems.	K2
CO2:	Explain the Automotive Transmission Control Systems.	K2
CO3:	Enumerate the principles, application, construction and specification of different sensors and actuators usable in typical automobile by suitable testing.	K2
CO4:	List out the principles and characteristics of charging system components and demonstrate their working with suitable tools.	K4
CO5:	Describe the principles and architecture of electronics systems and its components present in an automobile related to instrumentation, control, security and warning systems.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	2	2	3
CO2	-	-	1	3	-	2
CO3	3	-	3	3	1	2
CO4	-	-	2	3	3	3
CO5	-	-	1	3	1	2
Avg.	3	-	2	3	1	2

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2404	ROBOTICS					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• To Introduce the concepts of Robotic systems • To understand the concepts of Instrumentation and control related to Robotics • To understand the kinematics and dynamics of robotics • To explore robotics in Industrial applications					
UNIT – I	**INTRODUCTION TO ROBOTICS**					**9**
Robotics -History - Classification and Structure of Robotic Systems - Basic components -Degrees of freedom - Robot joints coordinates- Reference frames - workspace- Robot languages- Robotic sensors- proximity and range sensors, ultrasonic sensor, touch and slip sensor.						
UNIT – II	**ROBOT KINEMATICS AND DYNAMICS**					**9**
Kinematic Modelling: Translation and Rotation Representation, Coordinate transformation, DH parameters, Forward and inverse kinematics, Jacobian, Dynamic Modelling: Forward and inverse dynamics, Equations of motion using Euler-Lagrange formulation, Newton Euler formulation.						
UNIT – III	**ROBOTICS CONTROL**					**9**
Control of robot manipulator - state equations - constant solutions -linear feedback systems, singleaxis PID control - PD gravity control -computed torque control, variable structure control and impedance control.						
UNIT – IV	**ROBOT INTELLIGENCE AND TASK PLANNING**					**9**
Artificial Intelligence - techniques - search problem reduction - predicate logic means and end analysis - problem solving -robot learning - task planning - basic problems in task planning - AI in robotics and Knowledge Based Expert System in robotics						
UNIT – V	**INDUSTRIAL ROBOTICS**					**9**
Robot cell design and control - cell layouts - multiple robots and machine interference - work cell design - work cell control - interlocks – error detection deduction and recovery - work cell controller - robot cycle time analysis. Safety in robotics, Applications of robot and future scope.						
						Total: 45 periods
TEXT BOOK:						
1.	John J. Craig – Introduction to Robotics: Mechanics & Control (4th Ed., 2018)					
2.	M.P. Groover, M. Weiss, R.N. Nagel & N.G. Odrey – Industrial Robotics: Technology, Programming & Applications (McGraw-Hill, 2012)					
3.	**Mark W. Spong, Seth Hutchinson & M. Vidyasagar** – *Robot Modeling & Control* (Wiley, 2nd Ed., 2020)					
REFERENCES:						
1.	John J. Craig, 'Introduction to Robotics (Mechanics and Control)', Addison-Wesley, 2nd Edition, 2004.					
2.	Richard D. Klafter, Thomas A. Chmielewski, Michael Negin. 'Robotics Engineering: An					

	Integrated Approach', PHI Learning, New Delhi, 2009.
3.	K.S.Fu, R.C.Gonzalez and C.S.G.Lee, 'Robotics Control, Sensing, Vision and Intelligence', Tata McGraw Hill, 2nd Reprint,2008.
4.	Reza N.Jazar, 'Theory of Applied Robotics Kinematics, Dynamics and Control', Springer, 1 st Indian Reprint, 2010.
5.	Mikell. P. Groover, Michell Weis, Roger. N. Nagel, Nicolous G.Odrey, 'Industrial Robotics Technology, Programming and Applications ', McGraw Hill, Int 2012.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Describe the fundamentals of robotics	K2
CO2:	Understand the concept of kinematics and dynamics in robotics.	K2
CO3:	Discuss the robot control techniques	K2
CO4:	Explain the basis of intelligence in robotics and task planning	K4
CO5:	Discuss the industrial applications of robotics	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	3	-	3
CO2	-	-	1	3	-	3
CO3	-	-	1	3	-	3
CO4	-	-	1	3	-	2
CO5	2	-	1	3	-	3
Avg.	2	-	1	3	-	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPE2405	SOFT COMPUTING AND OPTIMIZATION TECHNIQUES					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• To classify various soft computing frame works. • To be familiar with the design of neural networks, fuzzy logic, and fuzzy systems. • To learn mathematical background for optimized genetic programming. • Be exposed to neuro-fuzzy hybrid systems and its applications. • To understand the various evolutionary optimization techniques.					
UNIT – I	**FUZZY LOGIC**					**9**
Introduction to Fuzzy logic - Fuzzy sets and membership functions- Operations on Fuzzy setsFuzzy relations, rules, propositions, implications, and inferences- Defuzzification techniques- Fuzzy logic controller design- Some applications of Fuzzy logic.						
UNIT – II	**ARTIFICIAL NEURAL NETWORKS**					**9**
Supervised Learning: Introduction and how brain works, Neuron as a simple computing element, The perceptron, Back propagation networks: architecture, multilayer perceptron, back propagation learning-input layer, accelerated learning in multilayer perceptron, The Hopfield network, Bidirectional associative memories (BAM), RBF Neural Network. Unsupervised Learning: Hebbian Learning, Generalized Hebbian learning algorithm, Competitive learning, Self- Organizing Computational Maps: Kohonen Network.						
UNIT – III	**GENETIC ALGORITHM**					**9**
Genetic algorithm- Introduction - biological background - traditional optimization and search techniques - Genetic basic concepts - operators – Encoding scheme – Fitness evaluation – crossover - mutation - Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.						
UNIT – IV	**NEURO-FUZZY MODELING**					**9**
Adaptive Neuro-Fuzzy Inference Systems (ANFIS) – architecture - Coactive Neuro-Fuzzy Modeling, framework, neuron functions for adaptive networks – Data Clustering Algorithms – Rule base Structure Identification –Neuro-Fuzzy Control – the inverted pendulum system.						
UNIT – V	**CONVENTIONAL OPTIMIZATION TECHNIQUES**					**9**
Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradientconjugate gradient, Newton's Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method, external penalty function method.						
						Total: 45 periods
TEXT BOOK:						
1.	Mitchell Melanie, An Introduction to Genetic Algorithm, Prentice Hall, 1998.					
2.	Simon Haykins, Neural Networks: A Comprehensive Foundation, Prentice Hall International Inc, 1999.					
3.	Timothy J.Ross, Fuzzy Logic with Engineering Applications, McGraw-Hill, 1997.					
REFERENCES:						

1.	J.S.R.Jang, C.T. Sun and E.Mizutani, Neuro-Fuzzy and Soft Computing, PHI / Pearson Education 2004.
2.	David E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Addison wesley, 2009.
3.	George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applications,Prentice Hall, 1995.
4.	James A. Freeman and David M. Skapura, Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Edn., 2003.
5.	Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, Neuro-Fuzzy and Soft Computing, Prentice-Hall of India, 2003.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Develop application on different soft computing techniques like Fuzzy, GA and Neural network	K2
CO2:	Implement Neuro-Fuzzy and Neuro-Fuzz-GA expert system.	K2
CO3:	Implement machine learning through Neural networks.	K2
CO4:	Model Neuro Fuzzy system for clustering and classification.	K4
CO5:	Able to use the optimization techniques to solve the real world problems	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	3	1	3	1
CO2	3	-	3	1	3	1
CO3	3	-	3	1	3	1
CO4	3	-	3	1	3	1
CO5	3	-	3	1	3	1
Avg.	3	-	3	1	3	1

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2406	RF SYSTEM DESIGN					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• Be familiar with RF transceiver system design for wireless communications • Be exposed to design methods of receivers and transmitters used in communication systems • Design RF circuits and systems using an advanced design tool. • Exemplify different synchronization methods circuits and describe their block schematic and design criteria • Measure RF circuits and systems with a spectrum analyzer.					
UNIT – I	**BASICS OF RADIO FREQUENCY SYSTEM DESIGN**					**9**
Definitions and models of Linear systems and Non-linear system. Specification parameters: Gain, noise figure, SNR, Characteristic impedance, S-parameters, Impedance matching and Decibels. Elements of digital base band signalling: complex envelope of band pass signals, Average value, RMS value, Crest factor, Sampling, jitter, modulation techniques, filters, pulse shaping, EVM, BER, 38 sensitivity, selectivity, dynamic range and, adjacent and alternate channel power leakages						
UNIT – II	**RADIO ARCHITECTURES AND DESIGN CONSIDERATIONS**					**9**
Superheterodyne architecture, direct conversion architecture, Low IF architecture, band-pass sampling radio architecture, System Design Considerations for an Analog Frontend Receiver in Cognitive Radio Applications, Interference, Near, In-band & wide-band considerations.						
UNIT – III	**AMPLIFIER MODELING AND ANALYSIS**					**9**
Noise: Noise equivalent model for Radio frequency device, amplifier noise model, cascade performance, minimum detectable signal, performance of noisy systems in cascade. Non-Linearity: Amplifier power transfer curve, gain compression, AM-AM, AM-PM, polynomial approximations, Saleh model, Wiener model and Hammerstein model, intermodulation, Single and two tone analyses, second and third order distortions and measurements, SOI and TOI points, cascade performance of nonlinear systems.						
UNIT – IV	**MIXER AND OSCILLATOR MODELING AND ANALYSIS**					**9**
Mixers: Frequency translation mechanisms, frequency inversion, image frequencies, spurious calculations, principles of mixer realizations. Oscillators: phase noise and its effects, effects of oscillator spurious components, frequency accuracy, oscillator realizations: Frequency synthesizers, NCO.						
UNIT – V	**APPLICATIONS OF SYSTEMS DESIGN**					**9**
Multimode and multiband Superheterodyne transceiver: selection of frequency plan, receiver system and transmitter system design – Direct conversion transceiver: receiver system and transmitter system design.						
						Total: 45 periods
TEXT BOOK:						
1.	Robert Sobot – Wireless Communication Electronics: Introduction to RF Circuits & Design Techniques (Springer, 2012)					

2.	Guillermo Gonzalez – Microwave Transistor Amplifiers: Analysis & Design
3.	Michael Steer – Fundamentals of Microwave and RF Design (2019, Open Textbook)
REFERENCES:	
1.	The Design of CMOS Radio-Frequency Integrated Circuits by Thomas H. Lee. Cambridge University Press, 2004.
2.	Qizheng Gu. "RF System Design of Transceivers for Wireless Communications", Springer ,2005.
3.	Kevin McClaning. "Wireless Receiver Design for Digital Communications," Yes Dee Publications, 2012.
4.	M C Jeruchim, P Balapan and K S Shanmugam, "Simulation of Communication systems:Modeling, Methodology and Techniques", Kluwer Academic/Plenum Publishers, 2 nd Edition, 2000.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Understand the specifications of transceiver modules	K2
CO2:	Understand pros and cons of transceiver architectures and their associated design considerations	K2
CO3:	Understand the impact of noise and amplifier non-linearity of amplification modules and also will learn the resultant effect during cascade connections	K2
CO4:	Get exposure about spurs and generation principles during signal generation and frequency translations	K4
CO5:	Understand the case study of transceiver systems and aid to select specification parameters	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	1	-	3
CO2	3	-	2	1	-	3
CO3	-	-	2	1	-	3
CO4	-	-	3	1	-	3
CO5	3	-	3	1	-	3
Avg.	3	-	3	1	-	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2407	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• To gain broad conceptual understanding of the various aspects of electromagnetic (EM)interference and compatibility • To develop a theoretical understanding of electromagnetic shielding effectiveness • To understand ways of mitigating EMI by using shielding, grounding and filtering • To understand the need for standards and to appreciate measurement methods • To understand how EMI impacts wireless and broadband technologies					
UNIT – I	**INTRODUCTION & SOURCES OF EM INTERFERENCE**					**9**
Introduction - Classification of sources - Natural sources - Man-made sources - Survey of the electromagnetic environment.						
UNIT – II	**EM SHIELDING**					**9**
Introduction - Shielding effectiveness - Far-field sources - Near-field sources - Low-frequency,magnetic field shielding - Effects of apertures						
UNIT – III	**INTERFERENCE CONTROL TECHNIQUES**					**9**
Equipment screening - Cable screening - grounding - Power-line filters - Isolation - Balancing - Signal-line filters - Nonlinear protective devices.						
UNIT – IV	**EMC STANDARDS, MEASUREMENTS AND TESTING**					**9**
Need for standards - The international framework - Human exposure limits to EM fields -EMC measurement techniques - Measurement tools - Test environments.						
UNIT – V	**EMC CONSIDERATIONS IN WIRELESS AND BROADB AND TECHNOLOGIES**					**9**
Efficient use of frequency spectrum - EMC, interoperability and coexistence - Specifications and alliances - Transmission of high-frequency signals over telephone and power networks – EMC and digital subscriber lines - EMC and power line telecommunications.						
						Total: 45 periods

REFERENCES:

1. Christopoulos C, Principles and Techniques of Electromagnetic Compatibility, CRC Press,Second Edition, Indian Edition, 2013.
2. Paul C R, Introduction to Electromagnetic Compatibility, Wiley India, Second Edition,2008.
3. Kodali V P, Engineering Electromagnetic Compatibility, Wiley India, Second Edition,2010.
4. Henry W Ott, Electromagnetic Compatibility Engineering, John Wiley & Sons Inc, Newyork,2009.

5.	Scott Bennett W, Control and Measurement of Unintentional Electromagnetic Radiation,John Wiley& Sons Inc., Wiley Interscience Series, 1997.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Demonstrate knowledge of the various sources of electromagnetic interference	K2
CO2:	Display an understanding of the effect of how electromagnetic fields couple throughapertures, and solve simple problems based on that understanding	K2
CO3:	Explain the EMI mitigation techniques of shielding and grounding	K2
CO4:	Explain the need for standards and EMC measurement methods	K4
CO5:	Discuss the impact of EMC on wireless and broadband technologies	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	-	-	3
CO2	-	-	1	-	-	2
CO3	-	-	1	-	-	3
CO4	-	-	1	-	2	3
CO5	-	-	1	-	-	3
Avg.	-	-	1	-	2	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2408	VLSI DESIGN TECHNIQUES					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• To understand the basics I-V characteristics of MOS transistor • To introduce the VLSI design flow • To Design combinational and sequential circuits • To introduce testing of VLSI circuits • To explore system design using Verilog HDL					
UNIT – I	**CMOS TECHNOLOGY**					**9**
MOS transistor, Ideal I–V characteristics, C–V characteristics, non-ideal I–V effects – CMOS Inverter and Pass transistor DC transfer characteristics – CMOS technologies, Layout design Rules – Stick Diagram – CMOS process enhancements– VLSI design Flow						
UNIT – II	**CIRCUIT DELAY,POWER,INTERCONNECT AND VERILOG HDL**					**9**
Delay estimation – Logical effort and Transistor sizing – Power dissipation – Interconnect – Design margin –Reliability – Scaling – SPICE – Device models. Verilog: Procedural assignments–conditionalstatements–Design of combinational and sequential circuits using different types of modeling –Test benches						
UNIT – III	**COMBINATIONAL AND SEQUENTIAL CIRCUIT DESIGN**					**9**
Circuit families –Circuit Pitfalls – Sequencing static circuits, Max-min delay constraints, Time borrowing, Clock Skew – circuit design of latches and flip flops – synchronizers, Meta stability, communication between asynchronous clock domains						
UNIT – IV	**CMOS TESTING**					**9**
Need for testing – Testers, Text fixtures and test programs – Logic verification – Silicon debug principles – Manufacturing test – Design for testability – Boundary scan test						
UNIT – V	**SYSTEM DESIGN USING VERILOG HDL**					**9**
Basic concepts- identifiers- gate primitives- gate delays- operators timing controls- procedural assignments-conditional statements- Design of combinational and sequential circuits using Data flow- structural gate level-switch level modeling and Behavioral modeling-Test benches						
						Total: 45 periods

REFERENCES:

1. Westeand Harris:"CMOS VLSI DESIGN"4thEdition,PearsonEducation,2013
2. Uyemura J.P:"Introduction toVLSI circuits ands ystems",Wiley2002
3. D.APucknell&K.Eshraghian,"Basic VLSI Design",3rdEdition,PHI,2003
4. WayneWolf,"Modern VLSI design",4theditionPearsonEducation,2009
5. M.J.S. Smith, "Application specific integrated circuits",1st edition, Addison-Wesley

	Professional,1997
6.	Ciletti,"Advanced Digital Design with the Verilog HDL",2ndedition,PearsonEducation 2010
7.	SamirPalnitkar" Verilog HDL a guide to digital design and Synthesis",PrenticeHall,2ndedition, 03

COURSE OUTCOMES: After the completion of the course the students will be able to		**BT Mapped (Highest Level)**
CO1:	Analyze the characteristics of CMOS transistor	K4
CO2:	Identify the methods to distribute clock and reduce power dissipation in CMOS circuits	K2
CO3:	Design combinational and sequential circuits	K2
CO4:	Analyze the methods to test the CMOS circuits	K4
CO5:	Synthesize the combinational and sequential circuits using Verilog HDL	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	2	-	3
CO2	1	-	2	1	-	2
CO3	2	-	1	2	1	3
CO4	-	-	1	2	1	2
CO5	1	-	1	2	3	3
Avg.	1	-	1	2	1	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPE2409	NANO TECHNOLOGIES					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• To introduce the basics of nano electronics • To understand the basics of semiconductor materials • To understand the basics of MOSFETS and its application in nano electronics • To learn the advanced nanoscale devices • To explore about Biosensors					
UNIT – I	**INTRODUCTION TO NANOELECTRONICS**					**9**
Introduction to nanoelectronics, Limitations of conventional microelectronics. Classical Particles, Classical Waves and Quantum Particles-Quantum Mechanics of Electronics -Schrödinger wave equation.						
UNIT – II	**MATERIALS FOR NANOELECTRONICS**					**9**
Introduction- Semiconductors, Crystal lattices: Bonding in crystals- Electron energy bands-Semiconductor heterostructures-Lattice-matched and pseudomorphic heterostructures-Carbon nanomaterials: nanotubes and fullerenes.						
UNIT – III	**SHRINK-DOWN APPROACHES**					9
Moore's Law- Technology Scaling and Reliability Challenges.Basic MOS Transistor-Types, Modes of operation, n-MOS operation, Drain Current, Threshold Voltage, Energy band diagram of MOSFET, nanoscale MOSFET, SCEs-limits to scaling, system integration limits.						
UNIT – IV	**ADVANCED NANOSCALE DEVICES**					**9**
Double Gate MOSFETs, Tri-Gate MOSFETs, Tunnel FETs-Multi-Gate TFETs and Heterojunction TFETs- Graphene and Carbon Nanotube Transistors.						
UNIT – V	**FET BASED BIOSENSORS**					9
Principles- Components of biosensor-Classification of Biosensors based on transducers, FET based Biosensor- ion-sensitive field effect transistor-operation and fabrication-Characteristics and Performance.						
						Total: 45 periods
TEXT BOOK:						
1.						
REFERENCES:						
1.	G.W. Hanson, Fundamentals of Nanoelectronics, Pearson, 2009					
2.	Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, "Introduction to Nanoelectronics: Science,					

	Nanotechnology, Engineering, and Applications", Cambridge University Press 2011
3.	Kodali V P, Engineering Electromagnetic Compatibility, Wiley India, Second Edition,2010.
4.	Pierre R. Coulet, Loïc J. Blum, Biosensor Principles and Applications, CRC press-2019.
5.	Donald A. Neamen, "Semiconductor Physics and Devices Basic Principles", Third Edition, McGraw-Hill Higher- Education, 2003.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Understand the basic concepts of nano electronics and various aspects of nano electronics.	K2
CO2:	Summarize the basic knowledge of Semiconductor materials and carbon nano tubes	K2
CO3:	Understand the basic concepts of MOS scaling	K2
CO4:	understand the advanced nanoscale devices	K3
CO5:	Understand the Bio sensor devices	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	3	-	3
CO2	1	-	2	2	-	2
CO3	2	-	1	2	1	3
CO4	-	-	1	3	1	2
CO5	1	-	1	2	3	3
Avg.	1	-	1	3	1	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPE2410	VLSI TESTING					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• to introduce the VLSI testing. • to introduce logic and fault simulation and testability measures • to study the test generation for combinational and sequential circuits • to study the design for testability. • to study the fault diagnosis.					
UNIT – I	**INTRODUCTION TO TESTING**					**9**
Introduction – VLSI Testing Process and Test Equipment – Challenges in VLSI Testing - Test Economics and Product Quality – Fault Modeling – Relationship Among Fault Models.						
UNIT – II	**LOGIC & FAULT SIMULATION & TESTABILITY MEASURES**					**9**
Simulation for Design Verification and Test Evaluation – Modeling Circuits for Simulation – Algorithms for True Value and Fault Simulation – Scoap Controllability and Observability						
UNIT – III	**TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS**					9
Algorithms and Representations – Redundancy Identification – Combinational ATPG Algorithms – Sequential ATPG Algorithms – Simulation Based ATPG – Genetic Algorithm Based ATPG						
UNIT – IV	**DESIGN FOR TESTABILITY**					**9**
Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture – Built-in Self-Test – Random Logic Bist – DFT for Other Test Objectives.						
UNIT – V	**FAULT DIAGNOSIS**					9
Introduction and Basic Definitions – Fault Models for Diagnosis – Generation of Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis						
						Total: 45 periods
TEXT BOOK:						
1.						
REFERENCES:						
1.	Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, "VLSI Test Principles and Architectures", Elsevier, 2017					
2.	Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital,Memory & Mixed-Signal VLSI Circuits" , Kluwer Academic Publishers, 2017.					
3.	Niraj K. Jha and Sandeep Gupta, "Testing of Digital Systems", Cambridge University Press,					

	2017.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Understand VLSI Testing Process	K2
CO2:	Develop Logic Simulation and Fault Simulation	K2
CO3:	Develop Test for Combinational and Sequential Circuits	K2
CO4:	Understand the Design for Testability	K3
CO5:	Perform Fault Diagnosis.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	2	-	3
CO2	1	-	2	1	3	2
CO3	2	-	1	2	1	3
CO4	-	-	1	2	2	2
CO5	1	-	2	2	-	3
Avg.	1	-	1	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPE2411	EDGE ANALYTICS AND INTERNET OF THINGS					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• To Understand the basis for intersection of IOT and Edge Analytics • To Understand the IOT protocols and standards • To comprehend the use of Machine Learning in Edge Analytics • To gain understanding on the use of Deep Learning techniques for analytics • To gain insight into edge analytics models and deployment					
UNIT – I	**INTRODUCTION TO IOT**					**9**
Importance and Need for IoT - Application and Use cases of IoT - Overview of Industrial IoT - Intersection of IoT and Edge Analytics.						
UNIT – II	**IOT PROTOCOLS AND SYSTEMS**					**9**
IoT protocols and standards - Cloud IoT Infrastructure - Setup and program IoT device- Data Collection from IoT device.						
UNIT – III	**MACHINE LEARNING AND ARTIFICIAL INTELLIGENCE**					9
Introduction to Machine Learning and Artificial Intelligence - Overview of Deep Learning and Neural Networks- Introduction to Convolution Neural Networks.						
UNIT – IV	**AUTO ENCODERS AND ITS PROGRAMMING**					**9**
Introduction to Recurrent Neural Networks- Introduction to Auto Encoders- Programming Practice: Build Image Classifier, Build Anomaly Detector						
UNIT – V	**EDGE ANALYTICS**					9
Challenges with Edge Devices and Deployment - Need for Model Quantization Quantization Aware Training- Post Model Quantization- Programming Practice: Model quantization, Deploying model on Edge Devices						
						Total: 45 periods
TEXT BOOK:						
1.						
REFERENCES:						
1.	Honbo Zhou, "The Internet of Things in the Cloud: A Middleware Perspective", CRC Press, 2012.					
2.	P. Flach, "Machine learning: The art and science of algorithms that make sense of data‖, Cambridge University Press, 2012.					
3.	Anirudh Koul, Siddha Ganju, Meher Kasam, "Practical Deep Learning for Cloud, Mobile, and					

	Edge" O'Reilly Media, 2019.
4.	Dieter Uckelmann, Mark Harrison, Florian Michahelles, "Architecting the Internet of Things", Springer, 2011.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Use the foundational concepts in Edge Analytics for application design and development	K2
CO2:	Use IOT protocols in cloud environments.	K2
CO3:	Implement and use Machine Learning and Artificial Intelligence algorithms and tools	K2
CO4:	implement and use Deep Learning techniques for applications	K3
CO5:	Analyze Edge devices analytics models and and its challenges	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	2	-	3
CO2	1	-	2	1	3	2
CO3	2	-	1	2	3	3
CO4	-	-	1	2	3	2
CO5	1	-	1	2	2	3
Avg.	1	-	1	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPE2412	QUANTUM COMPUTING					
		Category	L	T	P	Credit
		PEC	3	0	0	3

Course objectives

- To introduce the building blocks of Quantum computers and highlight the paradigm changebetween conventional computing and quantum computing
- To understand the Quantum state transformations and the algorithms
- To understand entangled quantum subsystems and properties of entangled states
- To explore the applications of quantum computing

UNIT – I	QUANTUM BUILDING BLOCKS	9

The Quantum Mechanics of Photon Polarization, Single-Qubit Quantum Systems, Quantum State Spaces, Entangled States, Multiple-Qubit Systems, Measurement of Multiple-Qubit States, EPR Paradox and Bell's Theorem, Bloch sphere

UNIT – II	QUANTUM STATE TRANSFORMATIONS	9

Unitary Transformations, Quantum Gates, Unitary Transformations as Quantum Circuits, Reversible Classical Computations to Quantum Computations, Language for Quantum Implementations.

UNIT – III	QUANTUM ALGORITHMS	9

Computing with Superpositions, Quantum Subroutines, Quantum Fourier Transformations. Shor's Algorithm and Generalizations, Grover's Algorithm and Generalizations

UNIT – IV	ENTANGLED SUBSYSTEMS AND ROBUST QUANTUM COMPUTATION	9

Quantum Subsystems, Properties of Entangled States, Quantum Error Correction, Graph states and codes, CSS Codes, Stabilizer Codes, Fault Tolerance and Robust Quantum Computing

UNIT – V	QUANTUM INFORMATION PROCESSING	9

Limitations of Quantum Computing, Alternatives to the Circuit Model of Quantum Computation, Quantum Protocols, Building Quantum, Computers, Simulating Quantum Systems, Bell states. Quantum teleportation. Quantum Cryptography, no cloning theorem

Total: 45 periods

REFERENCES:

1. John Gribbin, Computing with Quantum Cats: From Colossus to Qubits, 2021
2. William (Chuck) Easttom, Quantum Computing Fundamentals, 2021
3. Parag Lala, Quantum Computing, 2019
4. Eleanor Rieffel and Wolfgang Polak, QUANTUM COMPUTING A Gentle Introduction, 2011

COURSE OUTCOMES: On completion of the course, the students will be able to	BT Mapped (Highest Level)

CO1:	Understand the basic principles of quantum computing.	K2
CO2:	Gain knowledge of the fundamental differences between conventional computing andquantum computing.	K2
CO3:	Understand several basic quantum computing algorithms	K2
CO4:	Understand the classes of problems that can be expected to be solved well by quantumcomputers.	K3
CO5:	Simulate and analyze the characteristics of Quantum Computing Systems.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	-	1	-
CO2	1	-	-	-	2	-
CO3	-	-	-	2	-	2
CO4	-	-	3	1	-	-
CO5	-	2	-	-	2	-
Avg.	1	2	3	2	2	2

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2413	VLSI FOR WIRELESS COMMUNICATION					
	Category	L	T	P	Credit	
	PEC	3	0	0	3	
Course objectives						
	• To understand the concepts of basic wireless communication concepts. • To study the parameters in receiver and low noise amplifier design. • To study the various types of mixers designed for wireless communication. • To study and design PLL and VCO. • To understand the concepts of transmitters and power amplifie					
UNIT – I	**COMMUNICATION CONCEPTS**					**9**
Introduction – Overview of Wireless systems – Standards – Access Methods – Modulation schemes – Classical channel – Wireless channel description – Path loss – Multipath fading – Standard Translation.						
UNIT – II	**RECEIVER ARCHITECTURE & LOW NOISE AMPLIFIERS**					**9**
Receiver front end – Filter design – Non-idealities – Design parameters – Noise figure & Input intercept point. LNA Introduction – Wideband LNA design – Narrow band LNA design: Impedance matching & Core amplifier						
UNIT – III	**MIXERS**					9
Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion – Noise - A Complete Active Mixer. Switching Mixer – Distortion, Conversion Gain & Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain, Distortion, Intrinsic & Extrinsic Noise in Single Ended Sampling Mixer.						
UNIT – IV	**FREQUENCY SYNTHESIZERS**					**9**
PLL – Phase detector – Dividers – Voltage Controlled Oscillators – LC oscillators – Ring Oscillators – Phase noise – Loop filters & design approaches – A complete synthesizer design example (DECT) – Frequency synthesizer with fractional divider						
UNIT – V	**TRANSMITTER ARCHITECTURES & POWER AMPLIFIERS**					9
Transmitter back end design – Quadrature LO generator – Power amplifier design.						
						Total: 45 periods
TEXT BOOK:						
1.						
REFERENCES:						
1.	Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.					
2.	B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998.					
3.	Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999.					
4.	Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI wireless design – Circuits &					

	Systems", Kluwer Academic Publishers, 2000.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Able to recollect basic wireless communication concepts	K2
CO2:	To understand the parameters in receiver and design a low noise amplifier	K2
CO3:	In a position to apply his knowledge on various types of mixers designed for wirelesscommunication	K2
CO4:	Design PLL and VCO	K3
CO5:	Understand the concepts of transmitters and utilize the power amplifiers in wirelesscommunication	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	2	-	-
CO2	-	-	-	-	3	2
CO3	-	-	2	-	-	1
CO4	-	-	-	1	2	-
CO5	-	-	-	-	2	2
Avg.	-	-	2	2	2	2

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2414	MICRO ELECTRO MECHANICAL SYSTEMS					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• To understand the operation of sensors and actuators • To understand the operation of major classes of MEMS devices/systems • To give the fundamentals of standard micro fabrication techniques and processes • To understand the unique demands, environments and applications of MEMS devices • To understand RF MEMS, Bio MEMS and MOEMS					
UNIT – I	**INTRODUCTION TO MEMS**					**9**
Intrinsic Characteristics of MEMS – Energy Domains and Transducers- Sensors and Actuators – Introduction to Micro fabrication - Silicon based MEMS processes – New Materials – Review of Electrical and Mechanical concepts in MEMS – Semiconductor devices – Stress and strain analysis – Flexural beam bending- Torsional deflection						
UNIT – II	**SENSORSANDACTUATORS**					**9**
Electrostatic sensors – Parallel plate capacitors – Applications – Interdigitated Finger capacitor- Piezoresistive sensors – Piezoresistive sensor materials - piezoelectric effects – piezoelectricmaterials- Stress analysis of mechanical elements – Thermal Sensing and Actuation – Thermalexpansion – Thermal couples – Thermal resistors – Thermal Bimorph - Applications – MagneticActuators – Micromagneticcomponents.						
UNIT – III	**MICROMACHINING**					**9**
Silicon Anisotropic Etching – Anisotrophic Wet Etching – Dry Etching of Silicon – Plasma Etching – Deep Reaction Ion Etching (DRIE) – Isotropic Wet Etching – Gas Phase Etchants – Case studies – Basic surface micro machining processes – Structural and Sacrificial Materials – Acceleration of sacrificial Etch – Striction and Antistriction methods – LIGA Process - Assembly of 3D MEMS – Foundry process.						
UNIT – IV	**POLYMER AND OPTICAL MEMS**					**9**
Polymers in MEMS – SU-8, PMMA, PDMS, Langmuir – Blodgett Films, Micro System fabrication – Photolithography – Ion implantation- Diffusion – Oxidation – Chemical vapour deposition – Etching- Optical MEMS – Lenses and Mirrors – Actuators for Active Optical MEMS.						
UNIT – V	**OVERVIEWOFMEMSAREAS**					**9**
Bonding techniques for MEMS : Surface bonding , Anodic bonding , Silicon - on - Insulator , wire bonding , Sealing – Assembly of micro systems- RF MEMS - switches, active and passive components, Bio MEMS - Microfluidics, Digital Micro fluidics, Ink jet printer,- MOEMS - optical switch, optical cross-connect, tunable VCSEL, micro bolometers.						

	Total: 45 periods
TEXT BOOK:	
1.	Expose the students to occupational environment related to semiconductor devices and MEMS
2.	Create opportunity for acquiring practical skills of various field instruments in the area of MEMS devices
3.	Manage the issues arising during the execution of projects related to MEMS.
REFERENCES:	
1.	StephenDSenturia,'MicrosystemDesign',SpringerPublication,2000.
2.	ChangLiu,'FoundationsofMEMS',PearsonEducationInc.,2012.
3.	Marc J. Madou, 'Fundamentals of Microfabrication: The Science of Miniaturization', SecondEdition,2002.
4.	Nadim Maluf," An Introduction to Micro Electro Mechanical System Design", Artech House,2000.
5.	MohamedGad-el-Hak,editor,"TheMEMSHandbook",CRCpressBacoRaton,2001.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Understand the working principles of micro sensors and actuators	K2
CO2:	Understand the application of scaling laws in the design of micro systems	K2
CO3:	Understand the typical materials used for fabrication of micro machines	K2
CO4:	Understand the principles of standard micro fabrication techniques	K4
CO5:	Appreciate the challenges in the design and fabrication of RF,Bio, and MOEMS systems	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	1	-	-
CO2	-	-	2	-	-	2
CO3	2	-	-	-	-	-
CO4	-	1	1	-	-	-
CO5	-	-	-	1	-	3
Avg.	2	1	2	1	-	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2415	HARDWARE SECURE COMPUTING					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• Describe the fundamental principles in Data security • Discuss the watermarking algorithms and its usage • Explain the physical attacks and Modular arithmetic security methods • Describe the memory based attacks and vulnerabilities using deceptive mechanisms • Discuss the methods of FPGA implementation of cryptographic algorithms					
UNIT – I	**INTRODUCTION TO CRYPTO ALGORITHMS**					**9**
Cryptography basics, Cryptographic algorithms - Symmetric Key algorithms, Public Key algorithms and Hash Algorithms, Data Encryption Standards, Advanced Encryption Standards, RSA, BowFish						
UNIT – II	**DESIGN INTELLECTUAL PROPERTY PROTECTION**					**9**
Introduction to IP Protection, Watermarking Basics, Watermarking Examples, Good Watermarks, Fingerprinting, Hardware Metering.						
UNIT – III	**PHYSICAL ATTACKS AND MODULAR EXPONENTIATION**					**9**
Physical Attacks (PA) Basics, Physical Attacks and Countermeasures, Building Secure Systems, Modular Exponentiation (ME) Basics, ME in Cryptography, ME Implementation and Vulnerability, Montgomery Reduction.						
UNIT – IV	**ATTACKSANDCOUNTER MEASURES**					**9**
Introduction to Side Channel Attacks, Memory Vulnerabilities and Cache Attacks, Power Analysis, More Attacks and Countermeasures, Modified Modular Exponentiation, Hardware Trojan (HT) and Trusted IC, Hardware Trojan Taxonomy, Hardware Trojan Detection Overview, Hardware Trojan Detection Methods, Trusted IC Design with HT Prevention.						
UNIT – V	**EMERGING TECHNOLOGIES**					**9**
FPGA Implementation of Crypto algorithms, Vulnerabilities and Countermeasures in FPGA Systems, Role of Hardware in Security and Trust, Physical Unclonable Functions (PUF) Basics, Reliability, Trust Platform Modules						
						Total: 45 periods
TEXT BOOK:						
1.	Expose the students to occupational environment related to semiconductor devices and MEMS					
2.	Create opportunity for acquiring practical skills of various field instruments in the area of MEMS devices					
3.	Manage the issues arising during the execution of projects related to MEMS.					
REFERENCES:						
1.	Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, Hardware Security: Design,					

	Threats,andSafeguards,CRC Press,2014
2.	Tehranipoor,Mohammad,Wang,IntroductiontoHardware SecurityandTrust,Springer,2011.
3.	TedHuffmire,HandbookofFPGADesignSecurity,Springer,2010.
4.	Stefan Mangard, Elisabeth Oswald, Thomas Popp, Power Analysis Attacks - Revealing theSecretsofSmartCards,Springer,2007.
5.	DougStinson,CryptographyTheoryandPractice,CRCPress,2018.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Understand the basics of Cryptography	K2
CO2:	Identify the mechanism of Data Integrity protection mechanisms	K2
CO3:	Analyse the counter measures for physical attacks and the use of Modular exponentiation	K2
CO4:	Study side channel attacks and Trojan-based attacks	K2
CO5:	Challenges in Realisation using VLSI implementations	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	2	-	3
CO2	1	-	2	1	-	2
CO3	2	-	1	2	1	3
CO4	-	-	1	2	1	2
CO5	1	-	1	2	3	3
Avg.	1	-	1	2	1	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPE2416	CAD FOR VLSI DESIGN					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• To Introduce The Vlsi Design Methodologies And Design Methods. • To Introduce Data Structures And Algorithms Required For Vlsi Design. • To Study Algorithms For Partitioning And Placement. • To Study Algorithms For Floor Planning And Routing. • To Study Algorithms For Modelling, Simulation And Synthesis.					
UNIT – I	**INTRODUCTION**					**9**
Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles – Review of VLSI Design Automation Tools						
UNIT – II	**DATA STRUCTURES AND BASIC ALGORITHMS**					**9**
Introduction to Data Structures and Algorithms – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization.						
UNIT – III	**ALGORITHMS FOR PARTITIONING AND PLACEMENT**					**9**
Layout Compaction – Problem Formulation – Algorithms for Constraint Graph Compaction – Partitioning – Placement – Placement Algorithms.						
UNIT – IV	**ALGORITHMS FOR FLOORPLANNING AND ROUTING**					**9**
Floorplanning – Problem Formulation – Floorplanning Algorithms – Routing – Area Routing – Global Routing – Detailed Routing.						
UNIT – V	**MODELLING,SIMULATIONANDSYNTHESIS**					**9**
Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – Binary Decision Diagrams – High Level Synthesis.						
						Total: 45 periods
TEXT BOOK:						
1.	Expose the students to occupational environment related to semiconductor devices and MEMS					
2.	Create opportunity for acquiring practical skills of various field instruments in the area of MEMS devices					
3.	Manage the issues arising during the execution of projects related to MEMS.					
REFERENCES:						
1.	SabihH.Gerez,"AlgorithmsforVLSIDesignAutomation",SecondEdition,Wiley-India,2017.					
2.	Naveeda.Sherwani,"AlgorithmsforVLSIPhysicalDesignAutomation",3rdEdition,Springer,2017.					
3.	CharlesJ.Alpert,DineshP.MehtaandSachinSSapatnekar,"HandbookofAlgorithmsforPhysicalDesign Automation,CRCPress,1stEdition,2.					

4.	N.a.Sherwani,"AlgorithmsforVLSIPhysicalDesignAutomation",KluwerAcademicPublishers,2002.
5.	SabihH.Gerez,"AlgorithmsforVLSIDesignAutomation",SecondEdition,Wiley-India,2017.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Use various VLSI design methodologies	K2
CO2:	Understand different data structures and algorithms required for VLSI design.	K2
CO3:	Develop algorithms for partitioning and placement.	K2
CO4:	Develop algorithms for floor planning and routing.	K2
CO5:	Design algorithms for modelling, simulation and synthesis.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	-	-	-
CO2	-	-	2	2	-	-
CO3	-	-	2	-	-	1
CO4	-	-	2	-	-	1
CO5	-	-	2	-	-	1
Avg.	-	-	2	2	-	1

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2417	SENSORS AND ACTUATORS					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• Understand static and dynamic characteristics of measurement systems. • Study various types of sensors. • Study different types of actuators and their usage. • Study State-of-the-art digital and semiconductor sensors.					
UNIT – I	**INTRODUCTION TO MEASUREMENT SYSTEMS**					**9**
Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction, performance characteristics: static and dynamic characteristics of measurement systems, zero-order, first- order, and second-order measurement systems and response.						
UNIT – II	**RESISTIVE AND REACTIVE SENSORS**					**9**
Resistive sensors: potentiometers, strain gages, resistive temperature detectors, magneto resistors, light-dependent resistors, Signal conditioning for resistive sensors: Wheatstone bridge, sensor bridge calibration and compensation, Instrumentation amplifiers, sources of interference and interference reduction, Reactance variation and electromagnetic sensors, capacitive sensors, differential, inductive sensors, linear variable differential transformers (LVDT), magneto elastic sensors, hall effect sensors, Signal conditioning for reactance-based sensors & application to LVDT.						
UNIT – III	**SELF-GENERATING SENSORS**					**9**
Self-generatingsensors:thermoelectricsensors,piezoelectricsensors,pyroelectricsensors,photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors:chopperandlow-driftamplifiers,offsetanddriftsamplifiers,electrometeramplifiers,chargeamplifiers,noise in amplifiers.						
UNIT – IV	**ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS**					**9**
Relays, Solenoid drive, Stepper Motors, Voice-Coil actuators, Servo Motors, DC motors and motor control, 4-to-20 mA Drive, Hydraulic actuators, variable transformers: synchros, resolvers, Inductosyn, resolver-to-digital and digital-to-resolver converters.						
UNIT – V	**DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS**					**9**
Digital sensors: position encoders, variable frequency sensors – quartz digital thermometer, vibrating wire strain gages, vibrating cylinder sensors, Sensors based on semiconductor junctions: thermometers based on semiconductor junctions, magneto diodes and magneto transistors, MOSFET transistors, CCD imaging sensors , ultrasonic sensors, fiber-optic sensors.						
						Total: 45 periods
TEXT BOOK:						
1.	Expose the students to occupational environment related to semiconductor devices and MEMS					

2.	Create opportunity for acquiring practical skills of various field instruments in the area of MEMS devices
3.	Manage the issues arising during the execution of projects related to MEMS.
REFERENCES:	
1.	Andrzej M. Pawlak SensorsandActuatorsinMechatronicsDesignandApplications,2006.
2.	D.Johnson,"ProcessControlInstrumentationTechnology",8thEd,2014,JohnWileyandSons.
3.	D.Patranabis,"SensorsandTransducers",TMH2003.
4.	E.O.Doeblin."MeasurementSystem:ApplicationsandDesign",McGrawHill publications.1996
5.	GrahamBrooker,IntroductiontoSensorsforrangingandimaging,Yesdee,2009.
6.	HermanK.P.Neubrat."InstrumentTransducers–AnIntroductiontoTheirPerformanceandDesign",OxfordUniversityPress.22,1999.
7	IanSinclair,SensorsandTransducers, Elsevier, 3rdEdition,2011.
8	JonWilson,"SensorTechnologyHandbook",Newne2004.
9	KevinJames,PCInterfacingandDataacquisition,Elsevier,2011.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Compare Actuators with various drive characteristics.	K2
CO2:	Evaluate digital sensors and semiconductor device sensors performance metrics.	K5
CO3:	Characterize the performance of Self-generating sensors.	K3
CO4:	Analyze the performance of self-generating Sensors.	K4
CO5:	Analyze the performance of resistive and reactive sensors.	K4

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	2	-	3
CO2	1	-	2	1	-	2
CO3	2	-	1	2	1	3
CO4	-	-	1	2	1	2
CO5	1	-	1	2	3	3
Avg.	1	-	1	2	1	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPE2418	SIGNAL INTEGRITY FOR HIGH SPEED DESIGN					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• To identify sources affecting the speed of digital circuits. • To introduce methods to improve the signal transmission characteristics					
UNIT – I	**SIGNALPROPAGATIONONTRANSMISSIONLINES**					**9**
Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.						
UNIT – II	**MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK**					**9**
Non-idealsignalreturnpaths–gaps,BGAfields,viatransitions,Parasiticinductanceandcapacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current,differential-modecurrent,Connectors						
UNIT – III	**NON-IDEAL EFFECTS**					**9**
Self-generatingsensors:thermoelectricsensors,piezoelectricsensors,pyroelectricsensors,photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors:chopperandlow-driftamplifiers,offsetanddriftsamplifiers,electrometeramplifiers,chargeamplifiers,noise in amplifiers.						
UNIT – IV	**POWER CONSIDERATIONS AND SYSTEM DESIGN**					**9**
SN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.						
UNIT – V	**CLOCK DISTRIBUTION AND CLOCK OSCILLATORS**					**9**
Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.						
						Total: 45 periods
TEXT BOOK:						
1.	Expose the students to occupational environment related to semiconductor devices and MEMS					
2.	Create opportunity for acquiring practical skills of various field instruments in the area of MEMS devices					
3.	Manage the issues arising during the execution of projects related to MEMS.					
REFERENCES:						
1.	H.W.JohnsonandM.Graham,High-SpeedDigitalDesign:AHandbookofBlackMagic,PrenticeHall,1993.					

2.	DouglasBrooks,SignalIntegrityIssuesandPrintedCircuitBoardDesign,PrenticeHallPTR,2003.
3.	S.Hall,G.Hall,andJ.McCall,High-SpeedDigitalSystemDesign:AHandbooofInterconnectTheoryand DesignPractices,Wiley-Interscience,2000.
4.	EricBogatin, Signal Integrity–Simplified, PrenticeHallPTR,2003.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
co1:	Identify sources affecting the speed of digital circuits.	K3
CO2:	Identify methods to improve the signal transmission characteristics	K3
CO3:	Characterise and model multi conductor transmission line	K3
CO4:	Analyse clock distribution system and understand its design parameters	K4
CO5:	Analyse non ideal effects of transmission line	K4

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	3	-	-	-
CO2	-	-	3	-	-	-
CO3	-	-	2	1	-	-
CO4	-	-	-	2	2	-
CO5	-	-	2	1	-	-
Avg.	-	-	3	1	2	-

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2419	CONSUMER ELECTRONICS					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• To acquaint the students with the construction, theory and operation of the basic electronic devices such as PN junction diode, Bipolar and Field Effect Transistors, Power control devices etc., • To know about the working principle of LED, LCD and other Opto-electronic devices. • To introduce the concept of Sensors and voice controls. • To provide the knowledge on Smart home devices. • To gain knowledge on current communication technology					
UNIT – I	**CONSUMER ELECTRONICS FUNDAMENTALS**					**9**
History of Electronic Devices- Vacuum Tubes, Transistors, Integrated Circuits- Moorse Law, Semiconductor Devices, Diodes, Rectifiers, Transistors, Logic Gates, Combinational Circuits, ADC, DAC and Microprocessors, Microprocessor Vs Microcontrollers, Microcontrollers in consumer electronics, Energy management, Intelligent Building Perspective.						
UNIT – II	**ENTERTAINMENT ELECTRONICS**					**9**
Audio systems: Construction and working principle of: Microphone, Loud speaker, AM and FM receiver, stereo, Home theatre. Display systems: CRT, LCD, LED and Graphics displays Video Players: DVD and Blue RAY. Recording Systems: Digital Cameras and Camcorders.						
UNIT – III	**SMART HOME - SENSORS**					**9**
Technology involved in Smart home, Home Virtual Assistants- Alexa and Google Home. Home Security Systems - Intruder Detection, Automated blinds, Motion Sensors, Thermal Sensors and Image Sensors, PIR, IR and Water Level Sensors.						
UNIT – IV	**HOME APPLIANCES**					**9**
Home Enablement Systems: RFID Home, Lighting control, Automatic Cleaning Robots, Washing Machines, Kitchen Electronics- Microwave, Dishwasher, Induction Stoves, Smart Refrigerators, Smart alarms, Smart toilet, Smart floor, Smart locks.						
UNIT – V	**INTRODUCTION TO SMART OS AND COMMUNICATION**					**9**
Introduction to Smart OS- Android and iOS. Video Conferencing Systems- Web/IP Camera, Video security, Internet Enabled Systems, Wi-Fi, IoT, Li-Fi, GPS and Tracking Systems. Cordless Telephones, Fax Machines, PDAs- Tablets, Smart Phones and Smart Watches.						
						Total: 45 periods
TEXT BOOK:						
1.	Expose the students to occupational environment related to semiconductor devices and MEMS					
2.	Create opportunity for acquiring practical skills of various field instruments in the area of MEMS devices					
3.	Manage the issues arising during the execution of projects related to MEMS.					

REFERENCES:	
1.	Thomas LFloyd "Electronic Devices" 10thEditionPearsonEducation Asia2018.
2.	JordanFrith,"SmartphonesasLocativeMedia",Wiley.2014.
3.	Dennis CBrewer,"Home Automation",Que Publishing 2013.
4.	Thomas M.Coughlin,"Digital Storage in Consumer Electronics", ElsevierandNewness2012.
5.	Nickvandome,Smart homes in easy steps, -Master smart technology for your home2018.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
co1:	Explain the V-I characteristic of diode, UJT and SCR. Describe the equivalence circuits of transistors.	K2
CO2:	Operate the basic electronic devices such as PN junction diode, Bipolar and Field Effect Transistors, Power control devices, LED,LCD and other Opto-electronic devices.	K2
CO3:	Gain knowledge on sensors and controls.	K2
CO4:	Emphasize the need for communication systems.	K2
CO5:	Explore the current Technology and apply on home applications.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	3	-	-	-
CO2	-	-	3	-	-	-
CO3	-	-	2	1	-	-
CO4	-	-	-	2	2	-
CO5	-	-	2	1	-	-
Avg.	-	-	3	1	2	-

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAPE2420	ADVANCED MICROPROCESSORS AND MICROCONTROLLERS ARCHITECTURES					
		Category	L	T	P	Credit
		PEC	3	0	0	3
Course objectives						
	• To expose the students to the fundamentals of microprocessor architecture. • To explore the high performance features in CISC architecture • To familiarize the high performance features in RISC architecture • To introduce the basic features in Motorola microcontrollers. • To enable the students to understand PIC Microcontroller					
UNIT – I	**MICROPROCESSOR ARCHITECTURE**					**9**
Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC						
UNIT – II	**HIGH PERFORMANCE CISC ARCHITECTURE–PENTIUM**					**9**
CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes – Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor						
UNIT – III	**HIGH PERFORMANCE RISC ARCHITECTURE–ARM**					**9**
Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor						
UNIT – IV	**MSP430 16-BIT MICROCONTROLLER**					**9**
The MSP430 Architecture- CPU Registers -Instruction Set, On-Chip Peripherals -MSP430 - Development Tools, ADC - PWM - UART - Timer Interrupts - System design using MSP430Microcontroller						
UNIT – V	**PIC MICROCONTROLLER**					**9**
CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter – PWM and introduction to C-Compilers.						
						Total: 45 periods

REFERENCES:

1.	Daniel Tabak.,."Advanced Microprocessors"McGrawHill.Inc.,1995
2.	JamesL. Antonakos, "The Pentium Microprocessor",PearsonEducation,1997
3.	SteveFurber, "ARM System–On–Chiparchitecture",AddisionWesley,2000
4.	Gene.H.Miller."Micro Computer Engineering",PearsonEducation,2003
5.	John.B.Peatman, "Design with PIC Micro controller",Prenticehall, 1997
6.	JohnH.Davis,"MSP430 Microcontroller basics",Eelsevier,2008
7.	James L. Antonakos,"An Introduction to the Intel family of Micro processors",Pearson Education1999
8.	Barry.B.Breg," The Intel Microprocessors Architecture, Programming and Interfacing", PHI,2002
9.	Valvano "Embedded Microcomputer Systems"ThomsonAsiaPVTLTDfirstreprint2001
10	Readings: Weblinks--www.ocw.mit.edu,www.arm.com

COURSE OUTCOMES: At the end of the course the student will be able to		BT Mapped (Highest Level)
CO1:	To understand the fundamentals of microprocessor architecture	K2
CO2:	To know and appreciate the high performance features in CISC architecture	K2
CO3:	To know and appreciate the high performance features in RISC architecture.	K2
CO4:	To perceive the basic features in Motorola microcontrollers	K2
CO5:	To interpret and understand PIC Microcontroller	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	1	3	-	-	-
CO2	-	-	2	-	-	-
CO3	-	-	2	1	-	-
CO4	-	-	3	-	-	-
CO5	-	-	2	1	-	-
Avg.	-	1	2	1	-	-

Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2421	BIOMEDICAL SIGNAL PROCESSING					
		Category	L	T	P	Credit
		PCC	3	0	0	3
Course objectives						
	• Describe the properties and suitable models of biomedical signals • Introduce the basic signal processing techniques in analyzing biomedical signals • Develop computational skills in filtering of biomedical signals • Develop an understanding on ECG signal compression algorithms • Develop an understanding on feature extraction of biomedical signals					
UNIT – I	**INTRODUCTION TO BIOMEDICAL SIGNALS**					**9**
Introduction to Biomedical Signals: The nature of Biomedical Signals, Examples of Biomedical Signals, Objectives and difficulties in Biomedical analysis. Electrocardiography: Basic electrocardiography, ECG leads systems, ECG signal characteristics. Signal Conversion :Simple signal conversion systems, Conversion requirements for biomedical signals, Signal conversion circuits						
UNIT – II	**SIGNAL AVERAGING**					**9**
Signal Averaging: Basics of signal averaging, signal averaging as a digital filter, a typical averager, software for signal averaging, limitations of signal averaging. Adaptive Noise Cancelling: Principal noise canceller model, 60-Hz adaptive cancelling using a sine wave model, other applications of adaptive filtering						
UNIT – III	**DATA COMPRESSION TECHNIQUES**					**9**
Data Compression Techniques: Turning point algorithm, AZTEC algorithm, Fan algorithm, Huffman coding, data reduction algorithms The Fourier transform, Correlation, Convolution, Power spectrum estimation, Frequency domain analysis of the ECG						
UNIT – IV	**CARDIOLOGICAL SIGNAL PROCESSING**					**9**
Cardiological signal processing: Basic Electrocardiography, ECG data acquisition, ECG lead system, ECG signal characteristics (parameters and their estimation), Analog filters, ECG amplifier, and QRS detector, Power spectrum of the ECG, Bandpass filtering techniques, Differentiation techniques, Template matching techniques, A QRS detection algorithm, Realtime ECG processing algorithm, ECG interpretation, ST segment analyzer, Portable arrhythmia monitor						
UNIT – V	**NEUROLOGICAL SIGNAL PROCESSING**					**9**
Neurological signal processing: The brain and its potentials, The electrophysiological origin of brain waves, The EEG signal and its characteristics (EEG rhythms, waves, and transients), Correlation. Analysis of EEG channels: Detection of EEG rhythms, Template matching for EEG, spike and wave detection						
						Total: 45 periods
REFERENCES:						
1.	Rangaraj M Rangayyan "Biomedical Signal Analysis – A case study approach" IEEE press					

	series in biomedical engineering, First Edition, 2002
2.	John G Proakis, Dimitris and G. Manolakis, "Digital Signal Processing Principles algorithms, applications" PHI Third Edition. 2006
3.	Willis J. Tompkins " Biomedical Digital Signal Processing", EEE, PHI, 2004
4.	D C Reddy "Biomedical Signal Processing: Principles and Techniques", Tata McGraw-Hill Publishing Co. Ltd, 2005
5.	J G Webster "Medical Instrumentation: Application & Design", John Wiley & Sons Inc., 2001

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Possess skills necessary to analyze ECG and EEG Signals	K4
CO2:	Apply classical and modern filtering techniques for ECG and EEG Signals	K3
CO3:	Apply classical and modern compression techniques for ECG and EEG Signals	K3
CO4:	Develop an understanding on ECG feature extraction	K6
CO5:	Develop an understanding on EEG feature extraction	K6

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	2	-	3
CO2	1	-	2	1	-	2
CO3	2	-	1	2	1	3
CO4	-	-	1	2	1	2
CO5	1	-	1	2	3	3
Avg.	1	-	1	2	1	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2422	MODELING AND SYNTHESIS WITH HDL					
		Category	L	T	P	Credit
		PCC	3	0	2	4
Course objectives						
	• To know the basic language features of Verilog HDL and its the role in digital logic design. • To know the behavioural modeling of combinational and sequential circuits. • To know the behavioural modeling of algorithmic state machines. • To know the synthesis of combinational and sequential descriptions. • To know the architectural features of programmable logic devices.					
UNIT – I	**INTRODUCTION TO LOGIC DESIGN WITH VERILOG**					**7**
Overview of Digital Design with Verilog HDL - Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block - **Basic Concept- Modules and Ports**: Module definition, port declaration, connecting ports, hierarchical name referencing. **Tasks and Functions**						
UNIT – II	**LEVELS OF MODELING**					**12**
Gate-Level Modeling :Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. **Dataflow Modeling:** Continuous assignments, delay specification, expressions, operators, operands, operator types. **Behavioral Modeling:** Structured procedures, initial and always, blocking and nonblocking statements, delay control, generate statement, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.						
UNIT – III	**DESIGN OF DIGITAL LOGIC USING HDL**					**12**
Design of combinational logic: adders, multiplexers, de-multiplexers,encoders and decoders,comparators,multipliers - **Design of Sequential logic** : Flip-flops, synchronous and Asynchronous counters, shift registers, Universal shift register,FSM and LFSR. **(Using various Levels of Modeling)**						
UNIT – IV	**LOGIC SYNTHESIS AND DESIGN FLOW**					**7**
Logic Synthesis with verilog HDL-Synthesis Design flow, RTL and Test Bench Modeling Techniques and Timing and Path Delay Modeling, Timing Checks, Switch Level Modeling						
UNIT – V	**PROGRAMMABLE LOGIC DEVICES**					**7**
Programmable logic devices, storage devices, programmable logic array programmable array logic, programmability of PLDs CPLDs.						
						Total: 45 periods

PRACTICAL EXERCISES: 30 PERIODS
1. Design Entry Using VHDL Or Verilog Using HDL Languages of i. Combinational Circuits Namely 8:1 Mux/Demux, Full Adder, 8-Bit Magnitude Comparator, Encoder/Decoder, Priority Encoder. ii. Sequential Circuits Namely D-FF, 4-Bit Shift Registers (SISO, SIPO, PISO, Bidirectional), 3-Bit Synchronous Counters.
2. Test Vector Generation And Timing Analysis of Sequential And Combinational Logic Design for exercise (1) above. 2. Synthesis, P&R and Post P&R Simulation of the Components Simulated In (1) Above.
3. FPGA Implementation of PCI Bus & Arbiter. . Verifying Design Functionality Using Either Chipscope Feature (Xilinx) /the Signal Tap Feature (Altera)/Other Equivalent Feature . Invoke the PLL And Demonstrate the Use of the PLL Module for Clock Generation in FPGAs.

REFERENCES:

1.	Samir Palnitkar - Verilog HDL, 2nd edition, Pearson Education, 2003.
2.	Michael D Ciletti - Advanced Digital Design with the VERILOG HDL, 2ND Edition, PHI,2009.
3.	Z Navabi - Verilog Digital System Design, 2nd Edition, McGraw Hill, 2005.
4.	Stephen Brown and Zvonko Vranesic - Fundamentals of Digital Logic with Verilog, 2nd Edition, TMH, 2008.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1:	Demonstrate knowledge on HDL design flow and digital circuits design.	K4
CO2:	Design and develop the combinational and sequential circuits using various modeling	K6
CO3:	Solving algorithmic state machines using hardware description language	K4
CO4:	Analyze the process of synthesizing the combinational and sequential descriptions	K4
CO5:	Know the advantages of programmable logic devices and their description in Verilog	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	2	-	2	-
CO2	1	-	-	2	3	-
CO3	3	-	2	-	3	-
CO4	-	-	2	1	3	2
CO5	2	-	1	2	-	1
Avg.	2	-	2	2	3	2

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2423	DEEP LEARNING					
		Category	L	T	P	Credit
		PCC	3	0	2	4

Course objectives	
	• Develop and Train Deep Neural Networks. • Develop a CNN, R-CNN, Fast R-CNN, Faster-R-CNN, Mask-RCNN for detection andrecognition • Build and train RNNs, work with NLP and Word Embeddings • The internal structure of LSTM and GRU and the differences between them • The Auto Encoders for Image Processing

UNIT – I	DEEP LEARNING CONCEPTS	6
Fundamentals about Deep Learning. Perception Learning Algorithms. Probabilistic modelling. Early Neural Networks. How Deep Learning different from Machine Learning. Scalars. Vectors. Matrixes, Higher Dimensional Tensors. Manipulating Tensors. Vector Data. Time Series Data. Image Data. Video Data.		

UNIT – II	NEURAL NETWORKS	9
About Neural Network. Building Blocks of Neural Network. Optimizers. Activation Functions. Loss Functions. Data Pre-processing for neural networks, Feature Engineering. Overfitting and Underfitting. Hyperparameters.		

UNIT – III	CONVOLUTIONAL NEURAL NETWORK	10
About CNN. Linear Time Invariant. Image Processing Filtering. Building a convolutional neural network. Input Layers, Convolution Layers. Pooling Layers. Dense Layers. Backpropagation Through the Convolutional Layer. Filters and Feature Maps. Backpropagation Through the Pooling Layers. Dropout Layers and Regularization. Batch Normalization. Various Activation Functions. Various Optimizers. LeNet, AlexNet, VGG16, ResNet. Transfer Learning with Image Data. Transfer Learning using Inception Oxford VGG Model, Google Inception Model, Microsoft ResNet Model. R-CNN, Fast R-CNN, Faster R-CNN, Mask-RCNN, YOLO		

UNIT – IV	NATURAL LANGUAGE PROCESSING USING RNN	10
About NLP & its Toolkits. Language Modeling . Vector Space Model (VSM). Continuous Bag of Words (CBOW). Skip-Gram Model for Word Embedding. Part of Speech (PoS) Global Co-occurrence Statistics–based Word Vectors. Transfer Learning. Word2Vec. Global Vectors for Word Representation GloVe. Backpropagation Through Time. Bidirectional RNNs (BRNN) . Long Short Term Memory (LSTM). Bi-directional LSTM. Sequence-to-Sequence Models (Seq2Seq). Gated recurrent unit GRU.		

UNIT – V	DEEP REINFORCEMENT & UNSUPERVISED LEARNING	10
About Deep Reinforcement Learning. Q-Learning. Deep Q-Network (DQN). Policy Gradient Methods. Actor-Critic Algorithm. About Autoencoding. Convolutional Auto Encoding. Variational Auto Encoding. Generative Adversarial Networks. Autoencoders for Feature Extraction. Auto Encoders for Classification. Denoising Autoencoders. Sparse Autoencoders		
		Total: 45 periods

LIST OF EXPERIMENTS:		30 PERIODS
1.	Feature Selection from Video and Image Data	
2.	Image and video recognition	

3.	Image Colorization
4.	Aspect Oriented Topic Detection & Sentiment Analysis

REFERENCES:	
1.	Deep Learning A Practitioner's Approach Josh Patterson and Adam Gibson O'Reilly Media, Inc.2017
2.	Learn Keras for Deep Neural Networks, Jojo Moolayil, Apress,2018
3.	Deep Learning Projects Using TensorFlow 2, Vinita Silaparasetty, Apress, 2020
4.	Deep Learning with Python, FRANÇOIS CHOLLET, MANNING SHELTER ISLAND,2017
5.	Pro Deep Learning with TensorFlow, Santanu Pattanayak, Apress,2017

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Feature Extraction from Image and Video Data	K4
CO2:	Implement Image Segmentation and Instance Segmentation in Images	K3
CO3:	Implement image recognition and image classification using a pretrained network (TransferLearning)	K3
CO4:	Traffic Information analysis using Twitter Data	K3
CO5:	Auto encoder for Classification & Feature Extraction	K6

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	-	2	-	-
CO2	-	-	-	3	-	-
CO3	2	-	2	3	-	-
CO4	3	-	2	3	2	-
CO5	2	-	3	2	2	-
Avg.	3	-	2	3	2	-

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

PAPE2425	PCB DESIGN					
		Category	L	T	P	Credit
		PCC	3	0	2	4
Course objectives						
	• Understand the need for PCB Design and steps involved in PCB Design and Fabricationprocess. • Familiarize Schematic and layout design flow using Electronic Design Automation (EDA)Tools. • Understand basic concepts of transmission line, crosstalk and thermal issues • Design (schematic and layout) PCB for analog circuits, digital circuits and mixed circuits. • Schematic creation & interpretation					
UNIT – I	**INTRODUCTION TO PRINTED CIRCUIT BOARD**					**9**
Introduction to Printed circuit board: fundamental of electronic components, basic electronic circuits, Basics of printed circuit board designing: Layout planning, general rules and parameters, ground conductor considerations, thermal issues, check and inspection of artwork.						
UNIT – II	**DESIGN RULES FOR PCB**					**9**
Design rules for PCB: Design rules for Digital circuit PCBs, Analog circuit PCBs, high frequency and fast pulse applications, Power electronic applications, Microwave applications, **PCB Technology Trends**: Multilayer PCBs. Multiwire PCB, Flexible PCBs, Surface mount PCBs, Reflow soldering, Introduction to High-Density Interconnection (HDI) Technology.						
UNIT – III	**INTRODUCTION TO ELECTRONIC DESIGN AUTOMATION (EDA) TOOLS FOR PCB DESIGNING**					**9**
Introduction to Electronic design automation(EDA) tools for PCB designing: Brief Introduction of various simulators,SPICE and PSPICE Environment, Selecting the Components Footprints as per design, Making New Footprints, Assigning Footprint to components, Net listing, PCB Layout Designing, Auto routing and manual routing. Assigning specific text (silkscreen) to design, Creating report of design, creating manufacturing data (GERBER) for design.						
UNIT – IV	**INTRODUCTION PRINTED CIRCUIT BOARD PRODUCTION TECHNIQUES**					**9**
Introduction printed circuit board production techniques: Photo printing, film-master production, reprographic camera, basic process for double sided PCBs photo resists, Screen printing process, plating, relative performance and quality control, Etching machines, Solders alloys, fluxes, soldering techniques, Mechanical operations						
UNIT – V	**PCB DESIGN FOR EMI/EMC**					**9**
PCB design for EMI/EMC: Subsystem/PCB Placement in an enclosure, Filtering circuit placement, decoupling and bypassing, Electronic discharge protection, Electronic waste; Printed circuit boards Recycling techniques, Introduction to Integrated Circuit Packaging and footprints, NEMA and IPC standards.						
Total: 45 periods						

SUGGESTED ACTIVITIES:	**30 PERIODS**

1.	Using any Electronic design automation (EDA) software, Practice following PCB Design steps (Open source EDA Tool KiCad Preferable or equivalent) Example circuit: Basic RCCircuit Schematic Design: Familiarization of the Schematic Editor, Schematic creation, Annotation, Netlist generation Layouts Design: Familiarization of Footprint Editor, Mappingof components, Creation of PCB layout Schematic Create new schematic components Create new component footprints.
2.	Fabricate single-sided PCB, mount the components and assemble in a cabinet for any oneof the circuits mentioned below.
3.	Regulator circuit using 7805.
4.	Astable or Monostable multivibrator using IC555
5.	RC Phase-shift or Wein-bridge Oscillator using transistor.
6.	4 bit binary /MOD N counter using D-Flip flops.
7.	Design a 8051 Development board having Power section consisting of IC7805, capacitor,resistor, headers, LED,Serial communication section consisting of MAX 232, Capacitors,DB9 connector, Jumper, LEDs, Reset & Input/ output sections consisting of89C51 Microcontroller, Electrolytic Capacitor, Resistor, Jumper, Crystal Oscillator, Capacitors.
8.	Touch plate switches – transistorized or 555 based
9.	Doorbell/cordless bell
10.	Clapping switch and IR switch
11.	Blinkers
12.	Cell charger, battery charger, mobile charger
13.	Fire/smoke/intruder alarm
14.	Liquid level controller
15.	Audio amplifiers

REFERENCES:	
1.	Printed circuit board design ,fabrication assembly and testing By R. S. Khandpur, TataMcGraw Hill 2006
2.	Printed Circuits Handbook, Sixth Edition,by Clyde F. Coombs, Jr, Happy T. Holden,Publisher: McGraw-Hill Education Year: 2016
3.	Complete PCB Design Using OrCAD Capture and PCB Editor,Kraig Mitzner Bob DoeAlexander Akulin Anton Suponin Dirk Müller, 2nd Edition 2009.
4.	Introduction to System-on-Package, Rao R ,Tummala,&MadhavanSwaminathan, McGrawHill, 2008
5.	EMC and Printed circuit board ,Design theory and layout, Mark I Montrose IEEE compatibility society
6.	Electronic Product Design Volume-I by S D Mehta, S Chand Publications
7.	Open source EDA Tool KiCad Tutorial: http://kicad-pcb.org/help/tutorials/
8.	PCB Fabrication user guide page: http://www.wikihow.com/Create-Printed-Circuit-Boards , http://www.siongboon.com/projects/2005-09-07_home_pcb_fabrication/ ,
9.	http://reprap.org/wiki/MakePCBInstructions#Making_PCBs_yourself
10.	PCB Fabrication at home(video): https://www.youtube.com/watch?v=mv7Y0A9YeUc,
11.	https://www.youtube.com/watch?v=imQTCW1yWkg

COURSE OUTCOMES: On completion of the course, the students will be able to	**BT Mapped (Highest Level)**

CO1:	Appreciate the necessity and evolution of PCB, types and classes of PCB.	K2
CO2:	Understand the steps involved in schematic, layout, fabrication and assembly process of PCBdesign.	K2
CO3:	Apply advanced techniques, skills and modern tools for designing and fabrication of PCBs.	K3
CO4:	Apply the knowledge and techniques to fabricate Multilayer, SMT and HDI PCB.	K3
CO5:	Design (schematic and layout) and fabricate PCB for simple circuits.	K6

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	-	-	2	-
CO2	-	-	-	2	-	-
CO3	2	-	-	3	3	1
CO4	-	-	-	3	2	-
CO5	-	-	-	-	2	1
Avg.	2	-	-	3	2	1

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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POE2401	IPR, BIOSAFETY AND ENTREPRENEURSHIP					
		Category	L	T	P	Credit
		OEC	3	0	0	3

UNIT – I	IPR	9

Intellectual property rights – Origin of the patent regime – Early patents act & Indian pharmaceutical industry – Types of patents – Patent Requirements – Application preparation filing and prosecution – Patentable subject matter – Industrial design, Protection of GMO's IP as a factor in R&D,IP's of relevance to biotechnology and few case studies.

UNIT – II	AGREEMENTS, TREATIES AND PATENT FILING PROCEDURES	9

History of GATT Agreement – Madrid Agreement – Hague Agreement – WIPO Treaties –Budapest Treaty – PCT – Ordinary – PCT – Conventional – Divisional and Patent of Addition – Specifications – Provisional and complete – Forms and fees Invention in context of "prior art" –Patent databases – Searching International Databases – Country-wise patent searches (USPTO,espacenet(EPO) – PATENT Scope (WIPO) – IPO, etc National & PCT filing procedure – Time frame and cost – Status of the patent applications filed – Precautions while patenting – disclosure/non-disclosure – Financial assistance for patenting – Introduction to existing schemes Patent licensing and agreement Patent infringement – Meaning, scope, litigation, case studies

UNIT – III	BIOSAFETY	9

Introduction – Historical Backround – Introduction to Biological Safety Cabinets – Primary Containment for Biohazards – Biosafety Levels – Biosafety Levels of Specific Microorganisms – Recommended Biosafety Levels for Infectious Agents and Infected Animals – Biosafety guidelines – Government of India.

UNIT – IV	GENETICALLY MODIFIED ORGANISMS	9

Definition of GMOs & LMOs – Roles of Institutional Biosafety Committee – RCGM – GEAC etc. for GMO applications in food and agriculture – Environmental release of GMOs – Risk Analysis – Risk Assessment – Risk management and communication – Overview of National Regulations and relevant International Agreements including Cartegana Protocol.

UNIT – V	ENTREPRENEURSHIP DEVELOPMENT	9

Introduction – Entrepreneurship Concept – Entrepreneurship as a career – Entrepreneurial personality – Characteristics of successful Entrepreneur – Factors affecting entrepreneurial growth –

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Entrepreneurial Motivation – Competencies – Mobility – Entrepreneurship Development Programmes (EDP) - Launching Of Small Enterprise - Definition, Characteristics – Relationship between small and large units – Opportunities for an Entrepreneurial career – Role of small enterprise in economic development – Problems of small scale industries – Institutional finance to entrepreneurs - Institutional support to entrepreneurs.	
Total: 45 periods	
REFERENCES:	
1.	Bouchoux, D.E., "Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets for the Paralegal", 3rd Edition, Delmar Cengage Learning, 2008.
2.	Fleming, D.O. and Hunt, D.L., "Biological Safety: Principles and Practices", 4th Edition, American Society for Microbiology, 2006.
3.	Irish, V., "Intellectual Property Rights for Engineers", 2nd Edition, The Institution of Engineering and Technology, 2005.
4.	Mueller, M.J., "Patent Law", 3rd Edition, Wolters Kluwer Law & Business, 2009.
5.	Young, T., "Genetically Modified Organisms and Biosafety: A Background Paper for Decision-Makers and Others to Assist in Consideration of GMO Issues" 1st Edition, World Conservation Union, 2004.

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POE2405	MACHINE LEARNING AND DEEP LEARNING					
		Category	L	T	P	Credit
		OEC	3	0	0	3
Course objectives						
	The course is aimed at • Understanding about the learning problem and algorithms • Providing insight about neural networks • Introducing the machine learning fundamentals and significance • Enabling the students to acquire knowledge about pattern recognition. • Motivating the students to apply deep learning algorithms for solving real life problems.					
UNIT – I	**LEARNING PROBLEMS AND ALGORITHMS**					**9**
Various paradigms of learning problems, Supervised, Semi-supervised and Unsupervised algorithms						
UNIT – II	**NEURAL NETWORKS**					**9**
Differences between Biological and Artificial Neural Networks - Typical Architecture, Common Activation Functions, Multi-layer neural network, Linear Separability, Hebb Net, Perceptron, Adaline, Standard Back propagation Training Algorithms for Pattern Association - Hebb rule and Delta rule, Hetero associative, Auto associative, Kohonen Self Organising Maps, Examples of Feature Maps, Learning Vector Quantization, Gradient descent, Boltzmann Machine Learning.						
UNIT – III	**MACHINE LEARNING – FUNDAMENTALS & FEATURE SELECTIONS & CLASSIFICATIONS**					**9**
Classifying Samples: The confusion matrix, Accuracy, Precision, Recall, F1- Score, the curse of dimensionality, training, testing, validation, cross validation, overfitting, under-fitting the data, early stopping, regularization, bias and variance. Feature Selection, normalization, dimensionality reduction, Classifiers: KNN, SVM, Decision trees, Naïve Bayes, Binary classification, multi class classification, clustering.						
UNIT – IV	**DEEP LEARNING: CONVOLUTIONAL NEURAL NETWORKS**					**9**
Feed forward networks, Activation functions, back propagation in CNN, optimizers, batch normalization, convolution layers, pooling layers, fully connected layers, dropout, Examples of CNNs.						
UNIT – V	**DEEP LEARNING: RNNS, AUTOENCODERS AND GANS**					**9**
State, Structure of RNN Cell, LSTM and GRU, Time distributed layers, Generating Text, Autoencoders: Convolutional Autoencoders, Denoising autoencoders, Variational autoencoders, GANs: The discriminator, generator, DCGANs						
						Total: 45 periods
REFERENCES:						
1.	J. S. R. Jang, C. T. Sun, E. Mizutani, Neuro Fuzzy and Soft Computing - A Computational Approach to Learning and Machine Intelligence, 2012, PHI learning					

2.	Deep Learning, Ian Good fellow, YoshuaBengio and Aaron Courville, MIT Press, ISBN:9780262035613, 2016.
3.	The Elements of Statistical Learning. Trevor Hastie, Robert Tibshirani and Jerome Friedman. Second Edition. 2009.
4.	Pattern Recognition and Machine Learning. Christopher Bishop. Springer. 2006.
5.	Understanding Machine Learning. Shai Shalev-Shwartz and Shai Ben-David. Cambridge University Press. 2017.

COURSE OUTCOMES: At the end of the course the student will be able to		**BT Mapped (Highest Level)**
CO1:	Illustrate the categorization of machine learning algorithms.	K2
CO2:	Compare and contrast the types of neural network architectures, activation functions	K2
CO3:	Acquaint with the pattern association using neural networks	K2
CO4:	Elaborate various terminologies related with pattern recognition and architectures of convolutional neural networks	K4
CO5:	Construct different feature selection and classification techniques and advanced neural network architectures such as RNN, Autoencoders, and GANs.	K2

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POE2406	IoT FOR SMART SYSTEMS				
	Category	L	T	P	Credit
	OEC	3	0	0	3

Course objectives

- To study about Internet of Things technologies and its role in real time applications.
- To introduce the infrastructure required for IoT
- To familiarize the accessories and communication techniques for IoT.
- To provide insight about the embedded processor and sensors required for IoT
- To familiarize the different platforms and Attributes for IoT

UNIT – I INTRODUCTION TO INTERNET OF THINGS

Overview, Hardware and software requirements for IOT, Sensor and actuators, Technology drivers, Business drivers, Typical IoT applications, Trends and implications.

UNIT – II IOT ARCHITECTURE

IoT reference model and architecture -Node Structure - Sensing, Processing, Communication, Powering, Networking - Topologies, Layer/Stack architecture, IoT standards, Cloud computing for IoT, Bluetooth, Bluetooth Low Energy beacons.

UNIT – III PROTOCOLS AND WIRELESS TECHNOLOGIES FOR IOT

PROTOCOLS:

NFC, SCADA and RFID, Zigbee MIPI, M-PHY, UniPro, SPMI, SPI, M-PCIe GSM, CDMA, LTE, GPRS, small cell.

Wireless technologies for IoT: WiFi (IEEE 802.11), Bluetooth/Bluetooth Smart, ZigBee/ZigBee Smart, UWB (IEEE 802.15.4), 6LoWPAN, Proprietary systems-Recent trends.

UNIT – IV IOT PROCESSORS

Services/Attributes: Big-Data Analytics for IOT, Dependability,Interoperability, Security, Maintainability.

Embedded processors for IOT :Introduction to Python programming -Building IOT with RASPERRY PI and Arduino.

UNIT – V CASE STUDIES

Industrial IoT, Home Automation, smart cities, Smart Grid, connected vehicles, electric vehicle charging, Environment, Agriculture, Productivity Applications, IOT Defense

Total: 45 periods

REFERENCES:

1.	ArshdeepBahga and VijaiMadisetti : A Hands-on Approach "Internet of Things",Universities Press 2015.
2.	Oliver Hersent , David Boswarthick and Omar Elloumi " The Internet of Things", Wiley,2016.
3.	Samuel Greengard, " The Internet of Things", The MIT press, 2015.
4.	Adrian McEwen and Hakim Cassimally"Designing the Internet of Things "Wiley,2014.
5.	Jean- Philippe Vasseur, Adam Dunkels, "Interconnecting Smart Objects with IP: The Next Internet" Morgan Kuffmann Publishers, 2010.
6.	Adrian McEwen and Hakim Cassimally, "Designing the Internet of Things", John Wiley and sons, 2014.
7.	Lingyang Song/DusitNiyato/ Zhu Han/ Ekram Hossain," Wireless Device-to-Device Communications and Networks, CAMBRIDGE UNIVERSITY PRESS,2015.
8.	OvidiuVermesan and Peter Friess (Editors), "Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems", River Publishers Series in Communication, 2013.
9.	Vijay Madisetti , ArshdeepBahga, "Internet of Things (A Hands on-Approach)", 2014.
10	Zach Shelby, Carsten Bormann, "6LoWPAN: The Wireless Embedded Internet", John Wiley and sons, 2009.

COURSE OUTCOMES: At the end of the course the student will be able to		**BT Mapped (Highest Level)**
CO1:	Analyze the concepts of IoT and its present developments.	K4
CO2:	Compare and contrast different platforms and infrastructures available for IoT	K4
CO3:	Explain different protocols and communication technologies used in IoT	K2
CO4:	Analyze the big data analytic and programming of IoT	K4
CO5:	Implement IoT solutions for smart applications	K6

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	1	3	-	-	-
CO2	-	-	2	-	-	-
CO3	-	-	2	1	-	-
CO4	-	-	3	-	-	-
CO5	-	-	2	1	-	-
Avg.	-	1	2	1	-	-

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

POE2408	CLOUD COMPUTING TECHNOLOGIES					
		Category	L	T	P	Credit
		OEC	3	0	0	3
Course objectives						
	· To gain expertise in Virtualization, Virtual Machines and deploy practical virtualization solution · To understand the architecture, infrastructure and delivery models of cloud computing. · To explore the roster of AWS services and illustrate the way to make applications in AWS · To gain knowledge in the working of Windows Azure and Storage services offered by Windows Azure · To develop the cloud application using various programming model of Hadoop and Aneka					
UNIT – I	**VIRTUALIZATION AND VIRTUALIZATION INFRASTRUCTURE**					**6**
Basics of Virtual Machines - Process Virtual Machines – System Virtual Machines –Emulation – Interpretation – Binary Translation - Taxonomy of Virtual Machines. Virtualization –Management Virtualization — Hardware Maximization – Architectures – Virtualization Management – Storage Virtualization – Network Virtualization- Implementation levels of virtualization – virtualization structure – virtualization of CPU, Memory and I/O devices – virtual clusters and Resource Management – Virtualization for data center automation (WASH) and Integrated Water Resources Management (IWRM) - Need and Importance of WASH						
UNIT – II	**CLOUD PLATFORM ARCHITECTURE**					**12**
Cloud Computing: Definition, Characteristics - Cloud deployment models: public, private, hybrid, community – Categories of cloud computing: Everything as a service: Infrastructure, platform, software- A Generic Cloud Architecture Design – Layered cloud Architectural Development Architectural Design Challenges						
UNIT – III	**AWS CLOUD PLATFORM - IAAS**					**9**
Amazon Web Services: AWS Infrastructure- AWS API- AWS Management Console - Setting up AWS Storage - Stretching out with Elastic Compute Cloud - Elastic Container Service for Kubernetes- AWS Developer Tools: AWS Code Commit, AWS Code Build, AWS Code Deploy, AWS Code Pipeline, AWS code Star - AWS Management Tools: Cloud Watch, AWS Auto Scaling, AWS control Tower, Cloud Formation, Cloud Trail, AWS License Manager						
UNIT – IV	**PAAS CLOUD PLATFORM**					**9**
Windows Azure: Origin of Windows Azure, Features, The Fabric Controller – First Cloud APP in Windows Azure- Service Model and Managing Services: Definition and Configuration, Service						

runtime API- Windows Azure Developer Portal- Service Management API- Windows Azure Storage Characteristics-Storage Services- REST API- Blops		
UNIT – V	**PROGRAMMING MODEL**	**9**
Introduction to Hadoop Framework - Mapreduce, Input splitting, map and reduce functions, specifying input and output parameters, configuring and running a job –Developing Map Reduce Applications - Design of Hadoop file system –Setting up Hadoop Cluster- Aneka: Cloud Application Platform, Thread Programming, Task Programming and Map-Reduce Programming in Aneka		
		Total: 45 periods

REFERENCES:

1.	Bernard Golden, Amazon Web Service for Dummies, John Wiley & Sons, 2013.
2.	Raoul Alongi, AWS: The Most Complete Guide to Amazon Web Service from Beginner to Advanced Level, Amazon Asia- Pacific Holdings Private Limited, 2019.
3.	Sriram Krishnan, Programming: Windows Azure, O'Reilly,2010.
4.	Rajkumar Buyya, Christian Vacchiola, S.Thamarai Selvi, Mastering Cloud Computing , MCGraw Hill Education (India) Pvt. Ltd., 2013.
5.	Danielle Ruest, Nelson Ruest, —Virtualization: A Beginner"s Guide ‖ , McGraw-Hill Osborne Media, 2009.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Employ the concepts of virtualization in the cloud computing	K3
CO2:	Identify the architecture, infrastructure and delivery models of cloud computing	K2
CO3:	Develop the Cloud Application in AWS platform	K6
CO4:	Apply the concepts of Windows Azure to design Cloud Application	K3
CO5:	Develop services using various Cloud computing programming models.	K6

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POE2409	PRINCIPLES OF MULTIMEDIA					
		Category	L	T	P	Credit
		OEC	3	0	0	3

Course objectives

- To get familiarity with gamut of multimedia and its significance
- To acquire knowledge in multimedia components.
- To acquire knowledge about multimedia tools and authoring.
- To acquire knowledge in the development of multimedia applications
- To explore the latest trends and technologies in multimedia

UNIT – I	INTRODUCTION	6

Introduction to Multimedia – Characteristics of Multimedia Presentation – Multimedia Components– Promotion of Multimedia Based Components – Digital Representation – Media and Data Streams – Multimedia Architecture – Multimedia Documents, Multimedia Tasks and Concerns, Production, sharing and distribution, Hypermedia, WWW and Internet, Authoring, Multimedia over wireless and mobile networks.

Suggested Activities:

1. Flipped classroom on media Components.
2. External learning – Interactive presentation.

Suggested Evaluation Methods:

1. Tutorial – Handling media components
2. Quizzes on different types of data presentation.

UNIT – II	ELEMENTS OF MULTIMEDIA	12

Text-Types, Font, Unicode Standard, File Formats, Graphics and Image data representations –data types, file formats, color models; video – color models in video, analog video, digital video, file formats, video display interfaces, 3D video and TV: Audio – Digitization, SNR, SQNR, quantization, audio quality, file formats, MIDI; Animation- Key Frames and Tweening, other Techniques, 2D and 3D Animation.

Suggested Activities:

1. Flipped classroom on different file formats of various media elements.
2. External learning – Adobe after effects, Adobe Media Encoder, Adobe Audition.

Suggested Evaluation Methods:

1. Demonstration on after effects animations.
2. Quizzes on file formats and color models.

UNIT – III	MULTIMEDIA TOOLS	9

Authoring Tools – Features and Types – Card and Page Based Tools – Icon and Object Based Tools –

Time Based Tools – Cross Platform Authoring Tools – Editing Tools – Painting and Drawing Tools – 3D Modeling and Animation Tools – Image Editing Tools – Sound Editing Tools – Digital Movie Tools.

Suggested Activities:

1. Flipped classroom on multimedia tools.
2. External learning – Comparison of various authoring tools.

Suggested Evaluation Methods:

1. Tutorial – Audio editing tool.
2. Quizzes on animation tools.

UNIT – IV	MULTIMEDIA SYSTEMS	9

Compression Types and Techniques: CODEC, Text Compression: GIF Coding Standards, JPEG standard – JPEG 2000, basic audio compression – ADPCM, MPEG Psychoacoustics, basic Video compression techniques – MPEG, H.26X – Multimedia Database System – User Interfaces – OS Multimedia Support – Hardware Support – Real Time Protocols – Play Back Architectures – Synchronization – Document Architecture – Hypermedia Concepts: Hypermedia Design – Digital Copyrights, Content analysis.

Suggested Activities:

1. Flipped classroom on concepts of multimedia hardware architectures.
2. External learning – Digital repositories and hypermedia design.

Suggested Evaluation Methods:

1. Quizzes on multimedia hardware and compression techniques.
2. Tutorial – Hypermedia design.

UNIT – V	MULTIMEDIA APPLICATIONS FOR THE WEB AND MOBILE PLATFORMS	9

ADDIE Model – Conceptualization – Content Collection – Storyboard–Script Authoring Metaphors – Testing – Report Writing – Documentation. Multimedia for the web and mobile platforms. Virtual Reality, Internet multimedia content distribution, Multimedia Information sharing – social media sharing, cloud computing for multimedia services, interactive cloud gaming. Multimedia information retrieval.

Suggested Activities:

1. External learning – Game consoles.
2. External learning – VRML scripting languages.

Suggested Evaluation Methods:

1. Demonstration of simple interactive games.
2. Tutorial – Simple VRML program.

Total: 45 periods

REFERENCES:

1.	Li, Ze-Nian, Drew, Mark, Liu, Jiangchuan, "Fundamentals of Multimedia", Springer, Third Edition, 2021.
2.	Prabhat K.Andleigh, Kiran Thakrar, "MULTIMEDIA SYSTEMS DESIGN", Pearson Education, 2015.

3.	Gerald Friedland, Ramesh Jain, "Multimedia Computing", Cambridge University Press, 2018. (digital book)
4.	Ranjan Parekh, "Principles of Multimedia", Second Edition, McGraw-Hill Education, 2017

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Handle the multimedia elements effectively.	K3
CO2:	Articulate the concepts and techniques used in multimedia applications.	K3
CO3:	Develop effective strategies to deliver Quality of Experience in multimedia applications.	K6
CO4:	Design and implement algorithms and techniques applied to multimedia objects.	K5
CO5:	Design and develop multimedia applications following software engineering models.	K6

POE2413	SUSTAINABLE MANAGEMENT					
		Category	L	T	P	Credit
		OEC	3	0	0	3
Course objectives						
	· To provide students with fundamental knowledge of the notion of corporate sustainability. · To determine how organizations impacts on the environment and socio-technical systems, the relationship between social and environmental performance and competitiveness, the approaches and methods.					
UNIT – I	**MANAGEMENT OF SUSTAINABILITY**					**9**
Management of sustainability -rationale and political trends: An introduction to sustainability management, International and European policies on sustainable development, theoretical pillars in sustainability management studies.						
UNIT – II	**CORPORATE SUSTAINABILITY AND RESPONSIBILITY**					**9**
Corporate sustainability parameter, corporate sustainability institutional framework, integration of ustainability into strategic planning and regular business practices, fundamentals of stakeholder engagement.						
UNIT – III	**SUSTAINABILITY MANAGEMENT: STRATEGIES AND APPROACHES**					**9**
Corporate sustainability management and competitiveness: Sustainability-oriented corporate strategies, markets and competitiveness, Green Management between theory and practice, Sustainable Consumption and Green Marketing strategies, Environmental regulation and strategic postures; Green Management approaches and tools; Green engineering: clean technologies and innovation processes; Sustainable Supply Chain Management and Procurement.						
UNIT – IV	**SUSTAINABILITY AND INNOVATION**					**9**
Socio-technical transitions and sustainability, Sustainable entrepreneurship, Sustainable pioneers in green market niches, Smart communities and smart specializations.						
UNIT – V	**SUSTAINABLE MANAGEMENT OF RESOURCES, COMMODITIES AND COMMONS**					**9**
Energy management, Water management, Waste management, Wild Life Conservation, Emerging trends in sustainable management, Case Studies.						
						Total: 45 periods
REFERENCES:						
1.	Daddi, T., Iraldo, F., Testa, Environmental Certification for Organizations and Products: Management, 2015					

2.	Christian N. Madu, Handbook of Sustainability Management 2012
3.	Petra Molthan-Hill, The Business Student's Guide to Sustainable Management: Principles and Practice, 2014
4.	Margaret Robertson, Sustainability Principles and Practice, 2014
5.	Peter Rogers, An Introduction to Sustainable Development, 2006

COURSE OUTCOMES: Upon completion of this course, the students will be able to:		**BT Mapped (Highest Level)**
CO1:	An understanding of sustainability management as an approach to aid in evaluating and minimizing environmental impacts while achieving the expected social impact.	K2
CO2:	An understanding of corporate sustainability and responsible Business Practices	K2
CO3:	Knowledge and skills to understand, to measure and interpret sustainabilityperformances. landscape system.	K2
CO4:	Knowledge of innovative practices in sustainable business and community management	K2
CO5:	Deep understanding of sustainable management of resources and commodities	K2

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POE2414	MICRO AND SMALL BUSINESS MANAGEMENT					
		Category	L	T	P	Credit
		OEC	3	0	0	3

Course objectives

- To familiarize students with the theory and practice of small business management.
- To learn the legal issues faced by small business and how they impact operations.

UNIT – I	INTRODUCTION TO SMALL BUSINESS	9

Creation, Innovation, entrepreneurship and small business - Defining Small Business –Role of Owner – Manager – government policy towards small business sector –elements of entrepreneurship –evolution of entrepreneurship –Types of Entrepreneurship – social, civic, corporate - Business life cycle - barriers and triggers to new venture creation – process to assist start ups – small business and family business.

UNIT – II	SCREENING THE BUSINESS OPPORTUNITY AND FORMULATING THE BUSINESS PLAN	9

Concepts of opportunity recognition; Key factors leading to new venture failure; New venture screening process; Applying new venture screening process to the early stage small firm Role planning in small business – importance of strategy formulation – management skills for small business creation and development.

UNIT – III	BUILDING THE RIGHT TEAM AND MARKETING STRATEGY	9

Management and Leadership – employee assessments – Tuckman's stages of group development The entrepreneurial process model - Delegation and team building - Comparison of HR management in small and large firms - Importance of coaching and how to apply a coaching model.Marketing within the small business - success strategies for small business marketing - customer delight and business generating systems, - market research, - assessing market performance- sales management and strategy - the marketing mix and marketing strategy.

UNIT – IV	FINANCING SMALL BUSINESS	9

Main sources of entrepreneurial capital; Nature of 'bootstrap' financing - Difference between cash and profit - Nature of bank financing and equity financing - Funding-equity gap for small firms. Importance of working capital cycle - Calculation of break-even point - Power of gross profit margin- Pricing for profit - Credit policy issues and relating these to cash flow management and profitability.

UNIT – V	VALUING SMALL BUSINESS AND CRISIS MANAGEMENT	9

Causes of small business failure - Danger signals of impending trouble - Characteristics of poorly performing firms - Turnaround strategies - Concept of business valuation - Different valuation measurements - Nature of goodwill and how to measure it - Advantages and disadvantages of buying an established small firm - Process of preparing a business for sale.

Total: 45 periods

REFERENCES:	
1.	Hankinson,A.(2000). "The key factors in the profile of small firm owner-managers that influence business performance. The South Coast Small Firms Survey, 1997-2000." Industrial andCommercial Training 32(3):94-98.
2.	Parker,R.(2000). "Small is not necessarily beautiful: An evaluation of policy support for small and medium-sized enterprise in Australia." Australian Journal of Political Science 35(2):239-253.
3.	Journal articles on SME's.

COURSE OUTCOMES: Upon completion of this course, the students will be able to:		BT Mapped (Highest Level)
CO1:	Familiarise the students with the concept of small business	K2
CO2:	In depth knowledge on small business opportunities and challenges	K2
CO3:	Ability to devise plans for small business by building the right skills and marketingstrategies	K2
CO4:	Identify the funding source for small start ups	K4
CO5:	Business evaluation for buying and selling of small firms	K2

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POE2415	INTELLECTUAL PROPERTY RIGHTS					
		Category	L	T	P	Credit
		OEC	3	0	0	3

Course objectives

- To understand intellectual property rights and its valuation.

UNIT – I	INTRODUCTION	9

Intellectual property rights - Introduction, Basic concepts, Patents, Copyrights, Trademarks, Trade Secrets, Geographic Indicators; Nature of Intellectual Property, Technological Research, Inventions and Innovations, History - the way from WTO to WIPO, TRIPS.

UNIT – II	PROCESS	9

New Developments in IPR, Procedure for grant of Patents, TM, GIs, Patenting under Patent Cooperation Treaty, Administration of Patent system in India, Patenting in foreign countries.

UNIT – III	STATUTES	9

International Treaties and conventions on IPRs, The TRIPs Agreement, PCT Agreement, The Patent Act of India, Patent Amendment Act (2005), Design Act, Trademark Act, Geographical Indication Act, Bayh- Dole Act and Issues of Academic Entrepreneurship.

UNIT – IV	STRATEGIES IN INTELLECTUAL PROPERTY	9

Strategies for investing in R&D, Patent Information and databases, IPR strength in India, Traditional Knowledge, Case studies.

UNIT – V	MODELS	9

The technologies Know-how, concept of ownership, Significance of IP in Value Creation, IPValuation and IP Valuation Models, Application of Real Option Model in Strategic Decision Making, Transfer and Licensing.

Total: 45 periods

REFERENCES:

1. V. Sople Vinod, Managing Intellectual Property by (Prentice hall of India Pvt.Ltd), 2006.
2. Primer, R. Anita Rao and Bhanoji Rao, Intellectual Property Rights, Lastain Book company.
3. Edited by Derek Bosworth and Elizabeth Webster, The Management of Intellectual Property, Edward Elgar Publishing Ltd., 2006.

COURSE OUTCOMES:		BT Mapped (Highest Level)
CO1:	Understanding of intellectual property and appreciation of he need to protect it	K2
CO2:	Awareness about the process of patenting	K2
CO3:	Understanding of the statutes related to IPR	K2
CO4:	Ability to apply strategies to protect intellectual property	K4
CO5:	Ability to apply models for making strategic decisions related to IPR	K2

POE2416	ETHICAL MANAGEMENT					
		Category	L	T	P	Credit
		OEC	3	0	0	3

Course objectives

- To help students develop knowledge and competence in ethical management and decisionmaking in organizational contexts.

UNIT – I	ETHICS AND SOCIETY	9

Ethical Management- Definition, Motivation, Advantages-Practical implications of ethical management. Managerial ethics, professional ethics, and social Responsibility-Role of culture and society's expectations- Individual and organizational responsibility to society and the community

UNIT – II	ETHICAL DECISION MAKING AND MANAGEMENT IN A CRISIS	9

Managing in an ethical crisis, the nature of a crisis, ethics in crisis management, discuss case studies, analyze real-world scenarios, develop ethical management skills, knowledge, and competencies. Proactive crisis management.

UNIT – III	STAKEHOLDERS IN ETHICAL MANAGEMENT	9

Stakeholders in ethical management, identifying internal and external stakeholders, nature of stakeholders, ethical management of various kinds of stakeholders: customers (product and service issues), employees (leadership, fairness, justice, diversity) suppliers, collaborators, business, community, the natural environment (the sustainability imperative, green management, Contemporary issues).

UNIT – IV	INDIVIDUAL VARIABLES IN ETHICAL MANJAGEMENT	9

Understanding individual variables in ethics, managerial ethics, concepts in ethical psychology- ethical awareness, ethical courage, ethical judgment, ethical foundations, ethical emotions/intuitions/intensity. Utilization of these concepts and competencies for ethical decision- making and management.

UNIT – V	PRACTICAL FIELD-GUIDE, TECHNIQUES AND SKILLS	9

Ethical management in practice, development of techniques and skills, navigating challenges and dilemmas, resolving issues and preventing unethical management proactively. Role modelling and creating a culture of ethical management and human flourishing.

Total: 45 periods

REFERENCES:

1. Brad Agle, Aaron Miller, Bill O' Rourke, The Business Ethics Field Guide: the essential companion to leading your career and your company, 2016.
2. Steiner & Steiner, Business, Government & Society: A managerial Perspective, 2011.
3. Lawrence & Weber, Business and Society: Stakeholders, Ethics, Public Policy, 2020.

COURSE OUTCOMES:	BT Mapped (Highest Level)

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CO1:	Role modelling and influencing the ethical and cultural context.	K2
CO2:	Respond to ethical crises and proactively address potential crises situations.	K2
CO3:	Understand and implement stakeholder management decisions.	K2
CO4:	Develop the ability, knowledge, and skills for ethical management.	K4
CO5:	Develop practical skills to navigate, resolve and thrive in management situations	K2

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POE2417	INTEGRATED WATER RESOURCES MANAGEMENT					
		Category	L	T	P	Credit
		PCC	3	0	0	3

Course objectives

- Students will be introduced to the concepts and principles of IWRM, which is inclusive of the economics, public-private partnership, water & health, water & food security and legal & regulatory settings.

UNIT – I	CONTEXT FOR IWRM	9

Water as a global issue: key challenges – Definition of IWRM within the broader context of development – Key elements of IWRM - Principles – Paradigm shift in water management - Complexity of the IWRM process – UN World Water Assessment - SDGs.

UNIT – II	WATER ECONOMICS	9

Economic view of water issues: economic characteristics of water good and services – Non-market monetary valuation methods – Water economic instruments – Private sector involvement in water resources management: PPP objectives, PPP models, PPP processes, PPP experiences through case studies.

UNIT – III	LEGAL AND REGULATORY SETTINGS	9

Basic notion of law and governance: principles of international and national law in the area of water management - Understanding UN law on non-navigable uses of international water courses – International law for groundwater management – World Water Forums – Global Water Partnerships - Development of IWRM in line with legal and regulatory framework.

UNIT – IV	WATER AND HEALTH WITHIN THE IWRM CONTEXT	9

Links between water and health: options to include water management interventions for health – Health protection and promotion in the context of IWRM – Global burden of Diseases - Health impact assessment of water resources development projects – Case studies.

UNIT – V	AGRICULTURE IN THE CONCEPT OF IWRM	9

Water for food production: 'blue' versus 'green' water debate – Water foot print - Virtual water trade for achieving global water and food security — Irrigation efficiencies, irrigation methods - current water pricing policy– scope to relook pricing.

Total: 45 periods

REFERENCES:

1. Cech Thomas V., Principles of water resources: history, development, management and policy. John Wiley and Sons Inc., New York. 2003.
2. Mollinga .P. etal " Integrated Water Resources Management", Water in South Asia Volume I, Sage Publications, 2006.
3. Technical Advisory Committee, Integrated Water Resources management, Technical Advisory Committee Background Paper No: 4. Global water partnership, Stockholm, Sweden. 2002.
4. Technical Advisory Committee, Dublin principles for water as reflected in comparative assessment of institutional and legal arrangements for Integrated Water Resources Management, Technical Advisory Committee Background paper No: 3. Global water partnership, Stockholm,

	Sweden. 1999.
5.	Technical Advisory Committee, Effective Water Governance". Technical Advisory Committee Background paper No: 7. Global water partnership, Stockholm, Sweden, 2003.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Describe the context and principles of IWRM; Compare the conventional and integrated ways of water management.	K2
CO2:	Select the best economic option among the alternatives; illustrate the pros and cons of PPP through case studies.	K4
CO3:	Apply law and governance in the context of IWRM.	K3
CO4:	Discuss the linkages between water-health; develop a HIA framework.	K6
CO5:	Analyse how the virtual water concept pave way to alternate policy options.	K4

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	2	-	3
CO2	1	-	2	1	-	2
CO3	2	-	1	2	1	3
CO4	-	-	1	2	1	2
CO5	1	-	1	2	3	3
Avg.	1	-	1	2	1	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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POE2418	WATER, SANITATION AND HEALTH					
		Category	L	T	P	Credit
		OEC	3	0	0	3
Course objectives						
	• Understand the accelerating health impacts due to the present managerial aspects andinitiatives in water and sanitation and health sectors in the developing scenario					
UNIT – I	**FUNDAMENTALS WASH**					**9**
Meanings and Definition: Safe Water- Health, Nexus: Water- Sanitation - Health and Hygiene – Equity issues-Water security - Food Security. Sanitation And Hygiene (WASH) and Integrated Water Resources Management (IWRM) - Need and Importance of WASH						
UNIT – II	**MANAGERIAL IMPLICATIONS AND IMPACT**					**9**
Third World Scenario – Poor and Multidimensional Deprivation--Health Burden in Developing Scenario -Factors contribute to water, sanitation and hygiene related diseases-Social: Social Stratification and Literacy Demography: Population and Migration- Fertility - Mortality-Environment: Water Borne-Water Washed and Water Based Diseases - Economic: Wage - Water and Health Budgeting -Psychological: Non-compliance - Disease Relapse - Political: Political Will						
UNIT – III	**CHALLENGES IN MANAGEMENT AND DEVELOPMENT**					**9**
Common Challenges in WASH - Bureaucracy and Users- Water Utilities -Sectoral Allocation:-Infrastructure- Service Delivery: Health services: Macro and Micro- level: Community and Gender Issues- Equity Issues - Paradigm Shift: Democratization of Reforms and Initiatives.						
UNIT – IV	**GOVERNANCE**					**9**
Public health -Community Health Assessment and Improvement Planning (CHA/CHIP)- Infrastructure and Investments on Water, (WASH) - Cost Benefit Analysis – Institutional Intervention-Public Private Partnership - Policy Directives - Social Insurance -Political Will vs Participatory Governance -						
UNIT – V	**INITIATIVES**					**9**
Management vs Development -Accelerating Development- Development Indicators -Inclusive Development-Global and Local- Millennium Development Goal (MDG) and Targets - Five Year Plans - Implementation - Capacity Building - Case studies on WASH.						
Total: 45 periods						
REFERENCES:						
1.	Bonitha R., Beaglehole R.,Kjellstorm, 2006, "Basic Epidemiology", 2nd Edition, World Health Organization					
2.	Van Note Chism, N. and Bickford, D. J. (2002), Improving the environment for learning: An expanded agenda. New Directions for Teaching and Learning, 2002: 91–98. doi: 10.1002/tl.83Improving the Environment for learning: An Expanded Agenda					
3.	National Research Council. *Global Issues in Water, Sanitation, and Health: Workshop Summary.*					

	Washington, DC: The National Academies Press, 2009.
4.	Sen, Amartya 1997. On Economic Inequality. Enlarged edition, with annex by James Foster and Amartya Sen, Oxford: Claredon Press, 1997.
5.	Inter sectoral Water Allocation Planning and Management, 2000, World Bank Publishers www. Amazon.com

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Capture to fundamental concepts and terms which are to be applied and understoodall through the study.	K4
CO2:	Comprehend the various factors affecting water sanitation and health through the lens of third world scenario.	K2
CO3:	Critically analyse and articulate the underlying common challenges in water, sanitationand health.	K4
CO4:	Acquire knowledge on the attributes of governance and its say on water sanitation andhealth	K2
CO5:	Gain an overarching insight in to the aspects of sustainable resource management inthe absence of a clear level playing field in the developmental aspects.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	1	2	-	3
CO2	1	-	2	1	-	2
CO3	2	-	1	2	1	3
CO4	-	-	1	2	1	2
CO5	1	-	1	2	3	3
Avg.	1	-	1	2	1	3

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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POE2420	BLOCK CHAIN TECHNOLOGIES					
		Category	L	T	P	Credit
		OEC	3	0	0	3
Course objectives						
	• This course is intended to study the basics of Block chain technology. • During this course the learner will explore various aspects of Block chain technology likeapplication in various domains. • By implementing, learners will have idea about private and public Block chain, and smartcontract.					
UNIT – I	**INTRODUCTION OF CRYPTOGRAPHY AND BLOCKCHAIN**					**9**
Introduction to Block chain, Block chain Technology Mechanisms & Networks, Block chain Origins, Objective of Block chain, Block chain Challenges, Transactions and Blocks, P2P Systems, Keys as Identity, Digital Signatures, Hashing, and public key cryptosystems, private vs. public Block chain.						
UNIT – II	**BITCOIN AND CRYPTOCURRENCY**					**9**
Introduction to Bit coin, The Bit coin Network, The Bit coin Mining Process, Mining Developments, Bit coin Wallets, Decentralization and Hard Forks, Ethereum Virtual Machine (EVM), Merkle Tree, Double-Spend Problem, Block chain and Digital Currency, Transactional Blocks, Impact of Block chain Technology on Crypto currency.						
UNIT – III	**INTRODUCTION TO ETHEREUM**					**9**
Introduction to Ethereum, Consensus Mechanisms, Metamask Setup, Ethereum Accounts,Transactions, Receiving Ethers, Smart Contracts.						
UNIT – IV	**INTRODUCTION TO HYPERLEDGER AND SOLIDITY PROGRAMMING**					**10**
Introduction to Hyper ledger, Distributed Ledger Technology & its Challenges, Hyper ledger & Distributed Ledger Technology, Hyper ledger Fabric, Hyper ledger Composer. Solidity - Language of Smart Contracts, Installing Solidity & Ethereum Wallet, Basics of Solidity, Layout of a Solidity Source File & Structure of Smart Contracts, General Value Types.						
UNIT – V	**BLOCKCHAIN APPLICATIONS**					**8**
Internet of Things, Medical Record Management System, Domain Name Service and Future of Block chain, Alt Coins. Coding of Speech Signals, Quadrature Mirror Filters, Over Sampling A/D and D/A Conversion.						
						Total: 45 periods
REFERENCES:						
1.	Imran Bashir, "Mastering Block chain: Distributed Ledger Technology, Decentralization, and Smart Contracts Explained", Second Edition, Packt Publishing, 2018.					
2.	Narayanan, J. Bonneau, E. Felten, A. Miller, S. Goldfeder, "Bitcoin and Crypto currency Technologies: A Comprehensive Introduction" Princeton University Press, 2016					

3.	Antonopoulos, Mastering Bit coin, O'Reilly Publishing, 2014.
4.	Antonopoulos and G. Wood, "Mastering Ethereum: Building Smart Contracts and Dapps", O'Reilly Publishing, 2018.
5.	D. Drescher, Block chain Basics. Apress, 2017.

COURSE OUTCOMES: After the completion of this course, student will be able to		**BT Mapped (Highest Level)**
CO1:	Understand and explore the working of Block chain technology	K2
CO2:	Analyze the working of Smart Contracts	K2
CO3:	Understand and analyze the working of Hyper ledger	K2
CO4:	Apply the learning of solidity to build de-centralized apps on Ethereum	K4
CO5:	Develop applications on Block chain	K2

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POE2423	ENERGY CONSERVATION AND MANAGEMENT IN DOMESTIC SECTORS					
		Category	L	T	P	Credit
		OEC	3	0	0	3

Course objectives

1. To learn the present energy scenario and the need for energy conservation.
2. To understand the different measures for energy conservation in utilities.
3. Acquaint students with principle theories, materials, and construction techniques to create energy efficient buildings.
4. To identify the energy demand and bridge the gap with suitable technology for sustainable habitat
5. To get familiar with the energy technology, current status of research and find the ways to optimize a system as per the user requirement

UNIT – I	ENERGY SCENARIO	9

Primary energy resources - Sectorial energy consumption (domestic, industrial and other sectors), Energy pricing, Energy conservation and its importance, Energy Conservation Act-2001 and its features – Energy star rating.

UNIT – II	HEATING, VENTILLATION & AIR CONDITIONING	9

Basics of Refrigeration and Air Conditioning – COP / EER / SEC Evaluation – SPV system design & optimization for Solar Refrigeration.

UNIT – III	LIGHTING, COMPUTER, TV	9

Specification of Luminaries – Types – Efficacy – Selection & Application – Time Sensors – Occupancy Sensors – Energy conservation measures in computer – Television – Electronic devices.

UNIT – IV	ENERGY EFFICIENT BUILDINGS	9

Conventional versus Energy efficient buildings – Landscape design – Envelope heat loss and heat gain – Passive cooling and heating – Renewable sources integration.

UNIT – V	ENERGY STORAGE TECHNOLOGIES	9

Necessity & types of energy storage – Thermal energy storage – Battery energy storage, charging and discharging– Hydrogen energy storage & Super capacitors – energy density and safety issues – Applications.

Total: 45 periods

REFERENCES:

1. Yogi Goswami, Frank Kreith, Energy Efficiency and Renewable energy Handbook, CRC Press, 2016
2. ASHRAE Handbook 2020 – HVAC Systems & Equipment
3. Paolo Bertoldi, Andrea Ricci, Anibal de Almeida, Energy Efficiency in Household Appliances and Lighting, Conference proceedings, Springer, 2001
4. David A. Bainbridge, Ken Haggard, Kenneth L. Haggard, Passive Solar Architecture: Heating, Cooling, Ventilation, Daylighting, and More Using Natural Flows, Chelsea Green Publishing, 2011.

COURSE OUTCOMES: Upon completion of this course, the students will be able to:		BT Mapped (Highest Level)
CO1:	Understand technical aspects of energy conservation scenario.	K2
CO2:	Energy audit in any type for domestic buildings and suggest the conservation measures.	K4
CO3:	Perform building load estimates and design the energy efficient landscape system.	K4
CO4:	Gain knowledge to utilize an appliance/device sustainably.	K2
CO5:	Understand the status and current technological advancement in energy storage field.	K2

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POE2424	ADDITIVE MANUFACTURING					
		Category	L	T	P	Credit
		OEC	3	0	0	3
Course objectives						
	• This course is intended to study the basics of Additive Manufacturing. • During this course the learner will explore various design aspects of Additive Manufacturing. • By implementing, learners will deal with real time Case studies					
UNIT – I	**INTRODUCTION**					**9**
Need - Development - Rapid Prototyping Rapid Tooling – Rapid Manufacturing – Additive Manufacturing. AM Process Chain- Classification – Benefits.						
UNIT – II	**DESIGN FOR ADDITIVE MANUFACTURING**					**9**
CAD Model Preparation - Part Orientation and Support Structure Generation -Model Slicing - Tool Path Generation Customized Design and Fabrication - Case Studies.						
UNIT – III	**VAT POLYMERIZATION**					**9**
Stereolithography Apparatus (SLA)- Materials -Process -Advantages Limitations- Applications. Digital Light Processing (DLP) - Materials – Process - Advantages - Applications. Multi Jet Modelling (MJM) - Principles - Process - Materials - Advantages and Limitations.						
UNIT – IV	**MATERIAL EXTRUSION AND SHEET LAMINATION**					**9**
Fused Deposition Modeling (FDM)- Process-Materials - Applications and Limitations. Sheet Lamination Process: Laminated Object Manufacturing (LOM)- Basic Principle- Mechanism: Gluing or Adhesive Bonding – Thermal Bonding- Materials- Application and Limitation - Bio-Additive Manufacturing Computer Aided Tissue Engineering (CATE) – Case studies Selective Laser Sintering (SLS): Process –Mechanism– Typical Materials and Application- Multi Jet Fusion - Basic Principle-– Materials- Application and Limitation - Three Dimensional Printing - Materials -Process - Benefits and Limitations. Selective Laser Melting (SLM) and Electron Beam Melting (EBM): Materials – Process - Advantages and Applications. Beam Deposition Process: Laser Engineered Net Shaping (LENS)- Process -Material Delivery - Process Parameters - Materials - Benefits -Applications.						
UNIT – V	**CASE STUDIES AND OPPORTUNITIES ADDITIVE MANUFACTURING PROCESSES**					**9**
Education and training - Automobile- pattern and mould - tooling - Building Printing-Bio Printing - medical implants -development of surgical tools Food Printing -Printing Electronics. Business						

Opportunities and Future Directions - Intellectual Property.	
	Total: 45 periods
REFERENCES:	
1.	Andreas Gebhardt and Jan-Steffen Hötter "Additive Manufacturing: 3D Printing for Prototyping and Manufacturing", Hanser publications, United States, 2015, ISBN: 978-1- 56990-582-1..
2.	Ian Gibson, David W. Rosen and Brent Stucker "Additive Manufacturing Technologies: Rapid Prototyping to Direct Digital Manufacturing", 2nd edition, Springer., United States, 2015, ISBN13: 978-1493921126.
3.	Amit Bandyopadhyay and Susmita Bose, "Additive Manufacturing", 1st Edition, CRC Press., United States, 2015, ISBN-13: 978-1482223590
4.	Andreas Gebhardt, "Understanding Additive Manufacturing: Rapid Prototyping, Rapid Manufacturing", Hanser Gardner Publication, Cincinnati., Ohio, 2011, ISBN :9783446425521.
5.	Chua C.K., Leong K.F., and Lim C.S., "Rapid prototyping: Principles and applications", Third edition, World Scientific Publishers, 2010.

POE2425	ELECTRIC VEHICLE TECHNOLOGY					
		Category	L	T	P	Credit
		OEC	3	0	0	3

UNIT – I	NEED FOR ELECTRIC VEHICLES	9

History and need for electric and hybrid vehicles, social and environmental importance of hybrid and electric vehicles, impact of modern drive-trains on energy supplies, comparison of diesel, petrol, electric and hybrid vehicles, limitations, technical challenges

UNIT – II	ELECTRIC VEHICLE ARCHITECHTURE	9

Electric vehicle types, layout and power delivery, performance – traction motor characteristics, tractive effort, transmission requirements, vehicle performance, energy consumption, Concepts of hybrid electric drive train, architecture of series and parallel hybrid electric drive train, merits and demerits, mild and full hybrids, plug-in hybrid electric vehicles and range extended hybrid electric vehicles, Fuel cell vehicles.

UNIT – III	ENERGY STORAGE	9

Batteries – types – lead acid batteries, nickel based batteries, and lithium based batteries, electrochemical reactions, thermodynamic voltage, specific energy, specific power, energy efficiency, Battery modeling and equivalent circuit, battery charging and types, battery cooling, Ultra-capacitors, Flywheel technology, Hydrogen fuel cell, Thermal Management of the PEM fuel cell

UNIT – IV	ELECTRIC DRIVES AND CONTROL	9

Types of electric motors – working principle of AC and DC motors, advantages and limitations, DC motor drives and control, Induction motor drives and control, PMSM and brushless DC motor - drives and control , AC and Switch reluctance motor drives and control – Drive system efficiency – Inverters – DC and AC motor speed controllers

UNIT – V	DESIGN OF ELECTRIC VEHICLES	9

Materials and types of production, Chassis skate board design, motor sizing, power pack sizing, component matching, Ideal gear box – Gear ratio, torque–speed characteristics, Dynamic equation of vehicle motion, Maximum tractive effort – Power train tractive effort Acceleration performance, rated vehicle velocity – maximum gradability, Brake performance, Electronic control system, safety and challenges in electric vehicles. Case study of Nissan leaf, Toyota Prius, tesla model 3, and Renault Zoe cars.

Total: 45 periods

REFERENCES:

1. Iqbal Hussein, Electric and Hybrid Vehicles: Design Fundamentals, 2nd edition CRC Press, 2011.
2. Mehrdad Ehsani, Yimi Gao, Sebastian E. Gay, Ali Emadi, Modern Electric, Hybrid Electric andFuel Cell Vehicles: Fundamentals, Theory and Design, CRC Press, 2004.
3. James Larminie, John Lowry, Electric Vehicle Technology Explained - Wiley, 2003.
4. Ehsani, M, "Modern Electric, Hybrid Electric and Fuel Cell Vehicles: Fundamentals, Theory andDesign", CRC Press, 2005

PAXC2401	CONSTITUTION OF INDIA	

Category	L	T	P	Credit
AC	2	0	0	0

Course objectives		
	• Understand the premises in forming the twin themes of liberty and freedom from a civil rights perspective. • To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional • Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism. • To address the role of socialism in India after the commencement of the Bolshevik Revolution in1917and its impact on the initial drafting of the Indian Constitution	
UNIT – I	**HISTORY OF MAKING OF THE INDIAN CONSTITUTION**	**5**
History, Drafting Committee,(Composition & Working)		
UNIT – II	**PHILOSOPHY OF THE INDIAN CONSTITUTION**	**5**
Preamble, Salient Features		
UNIT – III	**CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES**	5
Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties		
UNIT – IV	**ORGANS OF GOVERNANCE**	**5**
Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions		
UNIT – V	**LOCAL ADMINISTRATION**	5
District's Administration head: Role and Importance, of Elected Representative, CEO, Municipal Corporation. Pachayatiraj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.		
UNIT – VI	**ELECTION COMMISSION**	5
Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.		
		Total: 30 periods

REFERENCES:

1. The Constitution of India,1950 (Bare Act),Government Publication
2. Dr.S.N.Busi, Dr.B.R. Ambedkar framing of Indian Constitution,1st Edition,2015

3.	M.P.Jain, Indian Constitution Law,7thEdn.,Lexis Nexis,2014.
4.	D.D.Basu,IntroductiontotheConstitutionofIndia,LexisNexis,2015.

COURSE OUTCOMES: Students will be able to		**BT Mapped (Highest Level)**
CO1:	Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics	K2
CO2:	Discuss the intellectual origins of the frame work of argument that informed the conceptualization of social reforms leading to revolution in India	K2
CO3:	Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.	K2
CO4:	Discuss the passage of the Hindu Code Bill of 1956	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	-	1	-
CO2	1	-	-	-	2	-
CO3	-	-	-	2	-	2
CO4	-	-	3	1	-	-
CO5	-	2	-	-	2	-
Avg.	1	2	3	2	2	2

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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PAXC2402	ENGLISH FOR RESEARCH PAPER WRITING				
	Category	L	T	P	Credit
	AC	2	0	0	0

Course objectives

- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission

UNIT – I	**INTRODUCTION TO RESEARCH PAPER WRITING**

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT – II	**PRESENTATION SKILLS**

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT – III	**TITLE WRITING SKILLS**

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

UNIT – IV	**RESULT WRITING SKILLS**

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT – V	**VERIFICATION SKILLS**

Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first- time submission

Total: 45 periods

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	Understand that how to improve your writing skills and level of readability	K2
CO2:	Learn about what to write in each section	K2
CO3:	Understand the skills needed when writing a Title	K2
CO4:	Understand the skills needed when writing the Conclusion	K2
CO5:	Ensure the good quality of paper at very first-time submission	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1
CO1	-	3	-	-	-	-	-	-	-	-	-	-	-
CO2	-	3	-	-	-	-	-	-	-	-	-	-	-
CO3	-	3	-	-	-	-	-	-	-	-	-	-	-
CO4	-	3	-	-	-	-	-	-	-	-	-	-	-
CO5	-	3	-	-	-	-	-	-	-	-	-	-	-
Avg.	-	3	-	-	-	-	-	-	-	-	-	-	-

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

PAXC2403	DISASTER MANAGEMENT				
	Category	L	T	P	Credit
	AC	2	0	0	0

Course objectives

- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches

UNIT – I	INTRODUCTION	6

Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT – II	REPERCUSSIONS OF DISASTERS AND HAZARDS	6

Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT – III	DISASTER PRONE AREAS IN INDIA	6

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics

UNIT – IV	DISASTER PREPAREDNESS AND MANAGEMENT	6

Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT – V	RISK ASSESSMENT	6

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival

Total: 30 periods

REFERENCES:

1. Disaster Administration And Management Text And Case Studies",Deep & Deep Publication Pvt. Ltd., New Delhi,2009.
2. NishithaRai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies

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	"'NewRoyal book Company,2007.
3.	Sahni, PardeepEt.Al. ," Disaster Mitigation Experiences And Reflections", Prentice Hall OfIndia, New Delhi,2001.

COURSE OUTCOMES: Students will be able to		**BT Mapped (Highest Level)**
CO1:	Ability to summarize basics of disaster	K2
CO2:	Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.	K2
CO3:	Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.	K2
CO4:	Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.	K2

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	-	1	-	1
CO2	-	-	1	2	-	1
CO3	-	-	1	2	1	-
CO4	-	-	1	2	2	-
CO5	-	-	1	2	-	-
Avg.	-	-	1	2	1	1

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

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